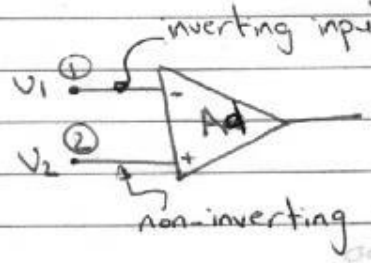
Electronics III

Most of the theory and equations mentioned in these lectures were taken from these following references:

- Adel S. Sedra, Kenneth C. Smith, “ Microelectronic Circuits “, 5th edition 2004.
- Donald A. Neamen, “ Microelectronic Circuit Analysis and design “, third edition 2007.
- Jacob Millman, Arvin Grabel, “Microelectronics “, second edition 1987.
- Clifton G. Fonstad, “MICROELECTRONIC DEVICES AND CIRCUITS” 2006

Operational amplifier:

The op-amp is a high gain direct coupled amplifier of which the first stage is a differential amplifier.



$v_o = A_d v_i$

$= A_d(v_2 - v_1)$

op-amp Symbol

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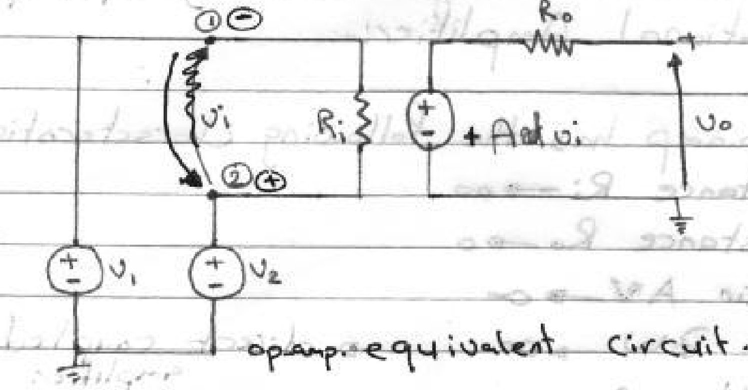


op-amp. equivalent circuit.

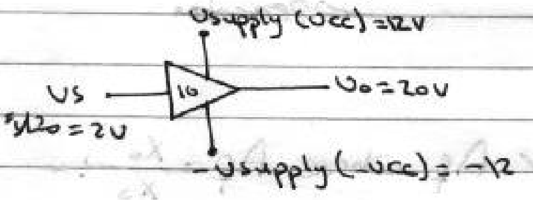
if $v_1 = 0$, then $v_o =$
$= + A_d v_2$

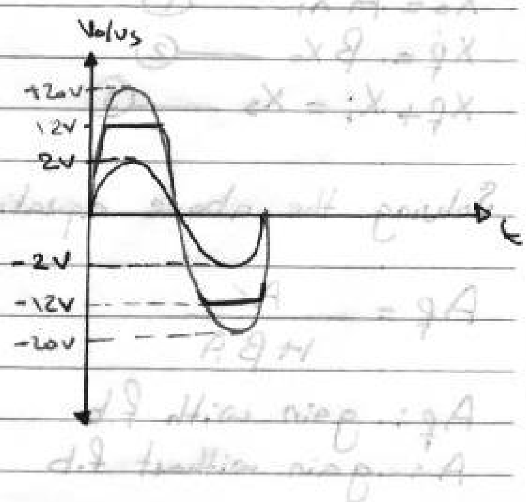
∴ terminal ② is the non-inverting terminal.

if $v_2 = 0$, then $v_o = - A_d v_1$

∴ terminal ① is the inverting terminal.

The op-amp is used to perform a wide variety of functions (operations).





أي ان فولتية الـ o/p لا يمكن الوصول
اليها في فولتية المصدر اذا أي ان
مستقطع الاشارة

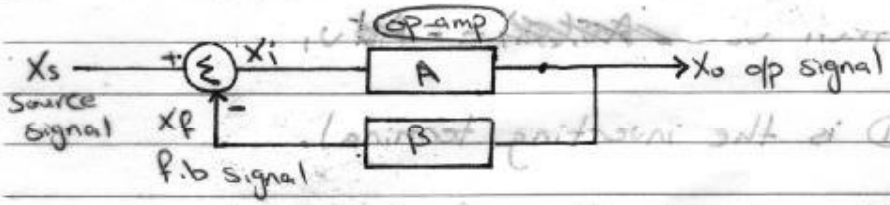
Date:

Ideal Operational Amplifier:-

The ideal op-amp has the following characteristics:-

1- Input resistance $R_i \to \infty$
2- Output resistance $R_o \to 0$
3- voltage gain $A_V \to \infty$
4- Bandwidth $BW \to \infty$
5- when $V_1 = V_2$, $V_o = 0$

$A_V \to \infty$ implies that $v_i = 0$. When the op-amp is used in linear applications. Such applications must employ negative feedback around the op-amp.



Block diagram of a negative feedback system

$X_o = A X_i$ — (1)

$X_f = \beta X_o$ — (2)

$X_f + X_i = X_s$ — (3)

Solving the above equations for A_f where $A_f = \frac{X_o}{X_s}$:-

$$A_f = \frac{A}{1 + \beta A}$$

A_f: gain with f.b
A: gain without f.b

$|A_f| < |A|$

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$$A_{f\,max} = \lim_{A\to\infty} A_f = \lim_{A\to\infty} \frac{1}{\frac{1}{A}+\beta} = \frac{1}{\beta} \text{ (finite value)}.$$

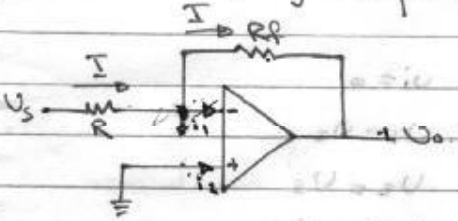
$\therefore X_o = A_f X_s$ is finite for a finite X_s

$$\therefore X_i = \frac{X_o}{A} = \frac{X_o(\text{finite})}{\infty} \to \frac{\text{finite}}{\infty} = 0$$

$A_V \to \infty$ must imply $v_i = 0$ for an ideal op-amp with -ve f.b. (linear applications).

Linear applications

1- Inverting amplifier



Since $R_i \to \infty$, $i_1 = 0$, $i_2 = 0$

The closed loop gain A_{vf} depends only on passive components, so A_{vf} is more accurate and predictable than A but smaller.

the current I through R also passes through Rf. In addition $A_V \to \infty$ implies $v_i = 0$ mentioned earlier so that the inverting terminal is effectively grounded. At the inverting input there exists a virtual ground or short circuit. The term virtual is used to imply that although the feedback from output to input through Rf serves to keep the voltage v_i at zero, no current actually flows into this short circuit as shown:-

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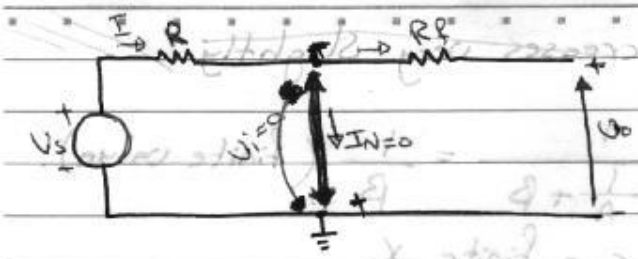
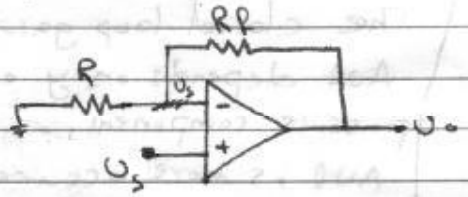


$$I = \frac{V_s}{R} = \frac{-V_o}{R_f}$$

$$\frac{V_o}{V_s} = \frac{-R_f}{R} = A_{vf} = \text{voltage gain with f.b.}$$

2- Non inverting amplifier:



$v_i = 0$

$\therefore v_1 = v_2$

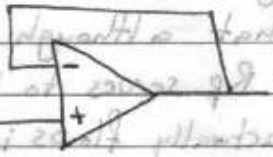
$v_2 = V_s$

$\therefore v_1 = V_s$

$$\frac{V_o - V_s}{R_f} = \frac{V_s}{R}$$

$$V_o - V_s = \frac{R_f}{R} V_s \Longrightarrow \frac{V_o}{V_s} = 1 + \frac{R_f}{R} = A_{vf}$$

if $R_f = 0$.



$\frac{V_o}{V_s} = 1$, $R_o = 0$, $R_i = \infty$

this is an op-amp as a buffer

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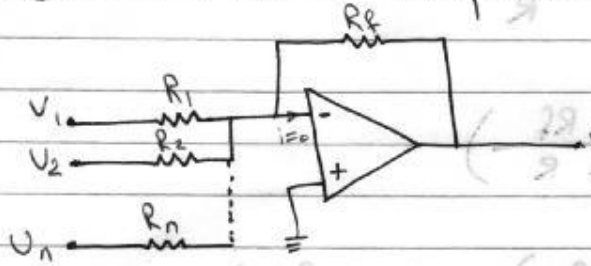
③ Summation Amplifier



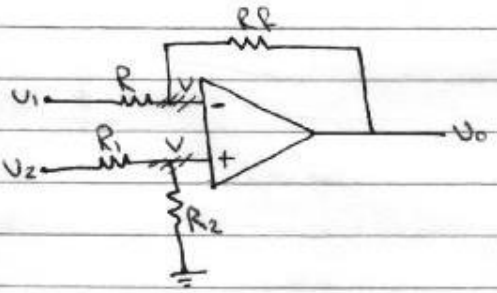
$$\frac{-V_o}{Rf} = \frac{V_1}{R_1} + \frac{V_2}{R_2} + \cdots + \frac{V_n}{R_n}$$

if $R_1 = R_2 = \cdots = R_n$

$$\frac{-V_o}{Rf} = \frac{1}{R_n}\left(V_1 + V_2 + \cdots + V_n\right)$$

$$V_o = \frac{-Rf}{R_n}\left(V_1 + V_2 + \cdots + V_n\right)$$

④ Difference Amplifier



$$V = V_2 \frac{R_2}{R_1 + R_2}$$

$$\frac{V_1 - V}{R} = \frac{V - V_o}{R_f} \longrightarrow \frac{V_1}{R} - \frac{V}{R} = \frac{V}{R_f} - \frac{V_o}{R_f}$$

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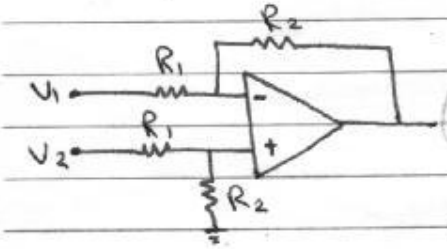
$$\frac{V_o}{R_f} = V\left(\frac{R_f + R}{R R_f}\right) - \frac{V_1}{R}$$

$$V_o = V\left(\frac{R_f + R}{R}\right) - V_1\left(\frac{R_f}{R}\right)$$

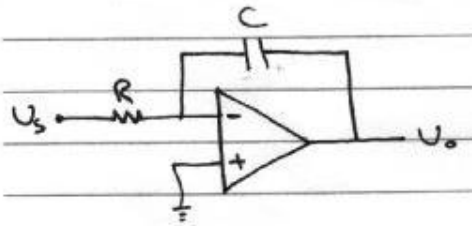
$$V_o = V_2\left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_f + R}{R}\right) - V_1\left(\frac{R_f}{R_1}\right)$$

if $R_f = R_2$ and $R = R_1$



$$V_o = \frac{R_2}{R_1}(V_2 - V_1)$$

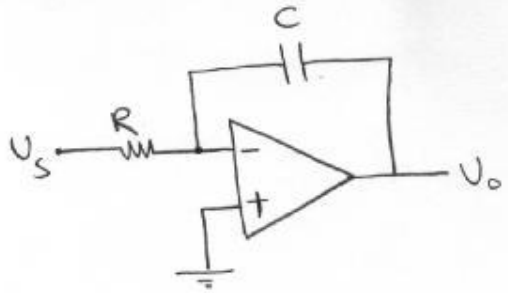
(5) Integrator :-



$$\frac{V_s}{R} = -C\frac{dv_o}{dt}$$

$$V_o = -\frac{1}{RC}\int_0^t V_s(x)\,dx$$

Miller Integrator:-



* At D.C ($\omega = 0$) the capacitor behaves as an open cct., there is no negative feedback.

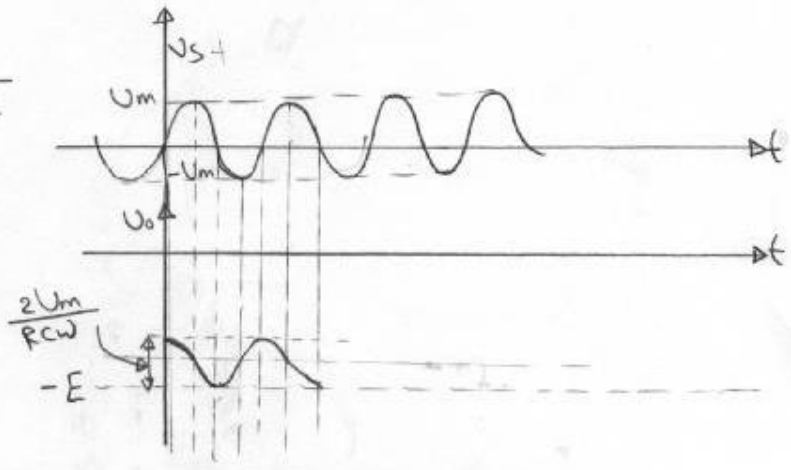
* This is very important in the integrator cct. and is a problem, because any tiny DC Component in the input signal will theoretically produce an infinite output. Ofcourse, no infinite o/p voltage results in practice, rather the o/p of the op-amp. Saturates at a voltage close to the op-amp. +ve or -ve power supply depending on the polarity of the input D.C signal.

$$\frac{V_o(j\omega)}{V_s(j\omega)} = \frac{-1}{j\omega RC}$$ (transfer c/c's of the Miller Integrator).

for example:-

$V_s = V_m \sin\omega t + \epsilon$, $\epsilon \to 0$ (ϵ is +ve)

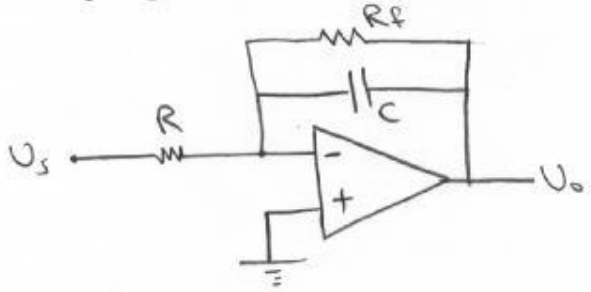
$$V_o = \frac{V_m}{RC\omega}\cos\omega t - \frac{\epsilon t}{RC}$$



E :- Saturation voltage of the op-amp.

To avoid this problem a resistor is added in parallel with the capacitor. If $R_f \gg X_c$ the new circuit will be as close to the Miller Integrator as possible.

The new circuit is called the D.C clamped integrator as shown below:-



$$\frac{V_o(j\omega)}{V_s(j\omega)} = \frac{-1}{\frac{R}{R_f} + j\omega RC}$$

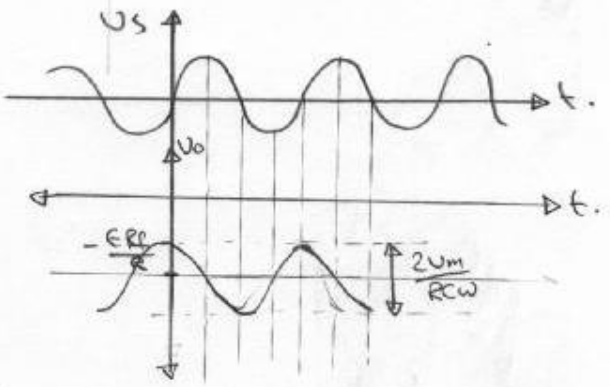
if $\omega = 0$ (D.C) then $\frac{V_o(j\omega)}{V_s(j\omega)} = -\frac{R_f}{R}$

if $\omega \neq 0$ the $\frac{V_o(j\omega)}{V_s(j\omega)} \approx \frac{-1}{j\omega RC}$ since $R_f \gg X_c$

For example:-

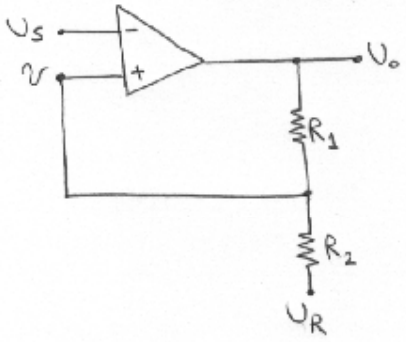
$V_s = \epsilon + V_m \sin\omega t$, $(\epsilon \to 0)$ ϵ is +ve

$V_o \approx -\epsilon \frac{R_f}{R} + \frac{V_m}{RC\omega} \cos\omega t$



Regenerative Comparator (schmitt trigger):-

(a) Inverting schmitt trigger



Assume that $V_s < v$ so that $V_o = +E$. The voltage v can be found by using superposition:-

$$v = V_R \frac{R_1}{R_1 + R_2} + V_o \frac{R_2}{R_1 + R_2}$$

In this case $v = V_R \frac{R_1}{R_1 + R_2} + E_o \frac{R_2}{R_1 + R_2} = V_1$

$= \text{Constant.}$

If V_s increases until $V_s = V_1$, then $V_o = -E$

The transfer c/c's of this case is as in figure (a).

<u>note:</u> E is the saturation voltage of the op-amp.

Now $V_o = -E$ and

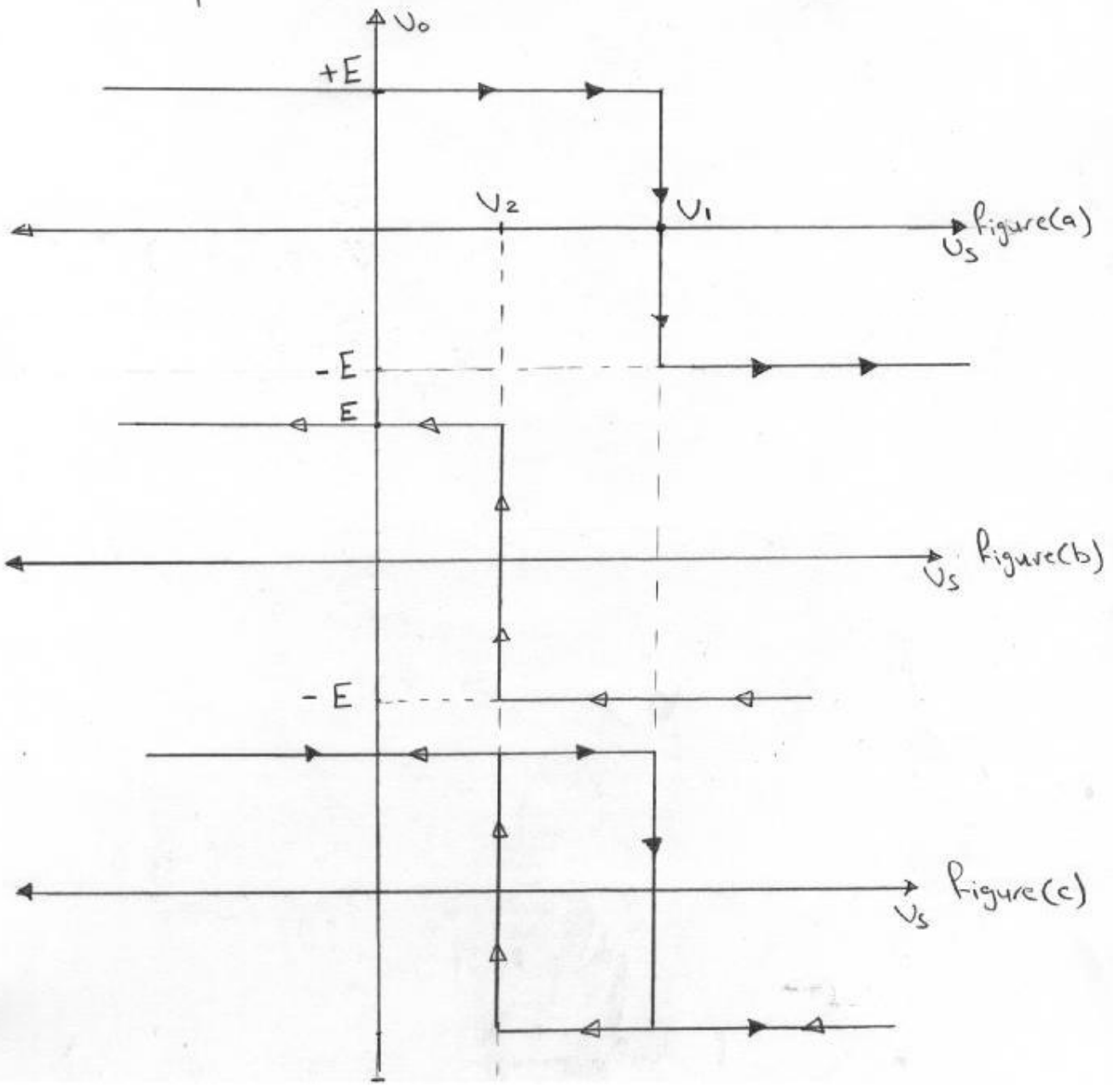
$$v = V_R \frac{R_1}{R_1+R_2} - E \frac{R_2}{R_1+R_2} = V_2 = \text{constant}$$

$V_2 < V_1$

If V_s decreases until $V_s = V_2$, then $V_o = +E$.

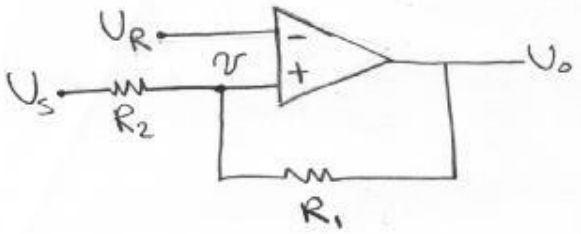
The transfer c/c's of this case is as in figure(b).

The Complete transfer c/c's is as in figure (c).



$V_H = V_1 - V_2 =$ Hysterisis

(b) Non - Inverting Schmitt trigger



Assume that $v < V_R$, $V_o = -E$,

$$v = V_s \frac{R_1}{R_1 + R_2} + V_o \frac{R_2}{R_1 + R_2}$$

In this case

$$v = V_s \frac{R_1}{R_1 + R_2} + -E \frac{R_2}{R_1 + R_2}$$

$$V_s \frac{R_1}{R_1 + R_2} - E \frac{R_2}{R_1 + R_2} < V_R$$

$$V_s < \left(V_R \frac{R_1 + R_2}{R_1} + E \frac{R_2}{R_1} \right) V_1$$

If V_s increases until $v \geq V_R$ and $V_s = V_1$, then $V_o = +E$. The transfer c/c's is as in figure (a).

Now $V_o = +E$ and

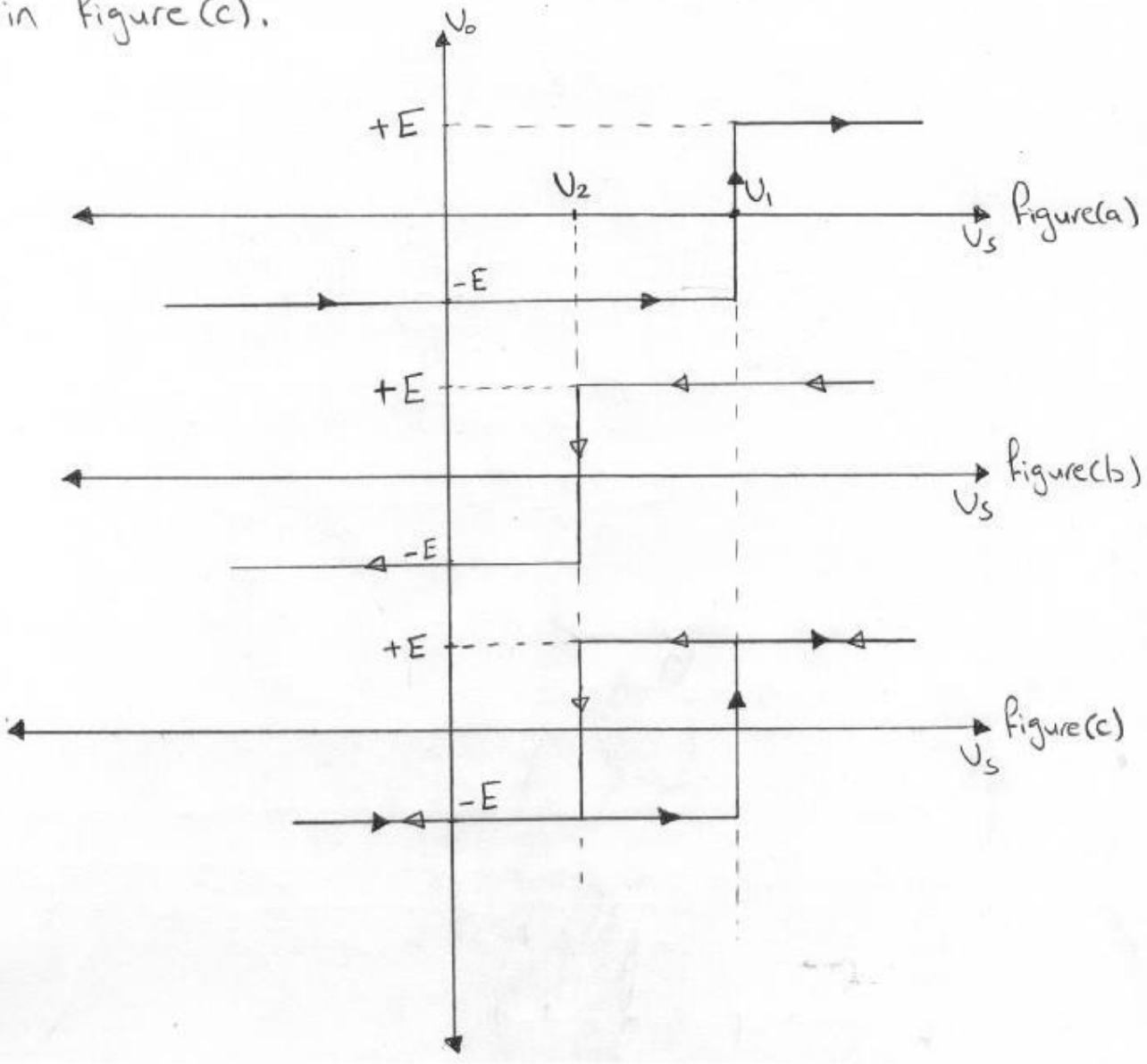
$$v = V_s \frac{R_1}{R_1 + R_2} + E \frac{R_2}{R_1 + R_2}$$

and

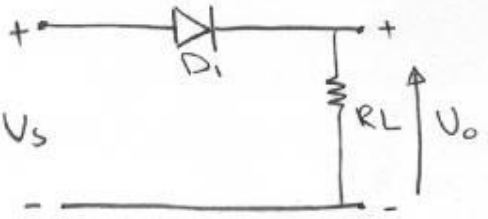
$$V_S \geq \left(V_R \frac{R_1+R_2}{R_2} - E \frac{R_1}{R_2}\right) \leftarrow V_2$$

If V_S decreases until $v \leq V_R$ and $V_S \leq V_2$ then $V_o = -E$

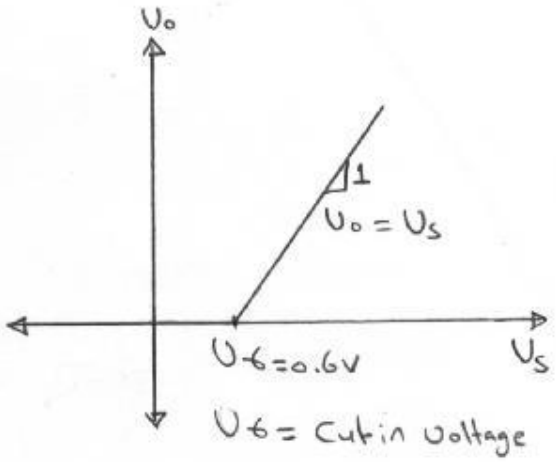
The transfer c/c's of this case is shown in figure (b). The Complete transfer c/c's is shown in figure (c).



Half-Wave Rectifier :-



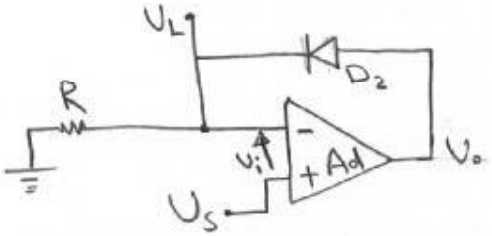
Half-Wave rectifier using a diode only.



V_γ = Cut-in voltage

if $V_s < 0.6\,V$, V_o = Zero.

So we will use the following circuit to rectify voltages less than 0.6 V:-



V_L :- the output of the rectifier

Half-wave rectifier using an op-amp.

Diode D_2 is not conducting when $V_o < V_\gamma$ and $V_L = 0$.

$$A_d = \frac{V_o}{V_i} \quad , \quad V_i = V_s - V_L$$

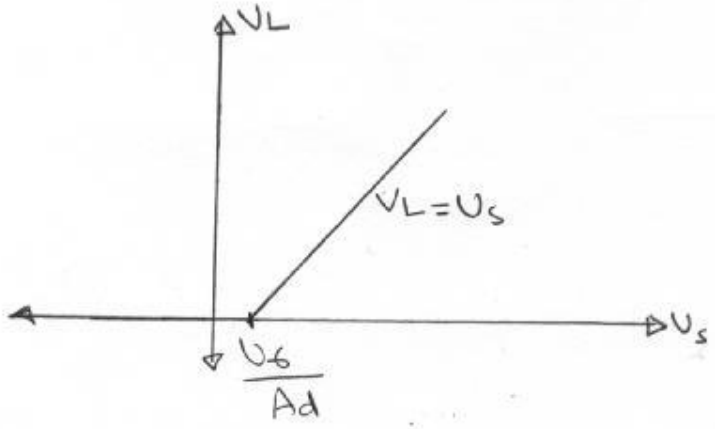
$$\therefore V_i = V_s$$

and $A_d V_s < V_\gamma$

$$V_s < \frac{V_\gamma}{A_d} \quad , \text{ typically } A_d = (10^5 - 10^6)$$

So if $V_S < 6\,\mu V$, $V_L = 0$.

Now if V_S increases until $V_o > V_\delta$ and $V_S > \frac{V_\delta}{A_d}$ then D_2 Conducts and $V_L = V_S$.



So Voltages in miliVolt range can be rectified

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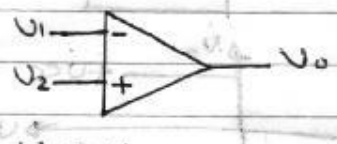
Non-linear applications:-

① The Comparator (limiter)

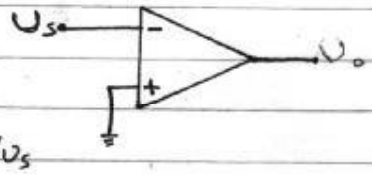


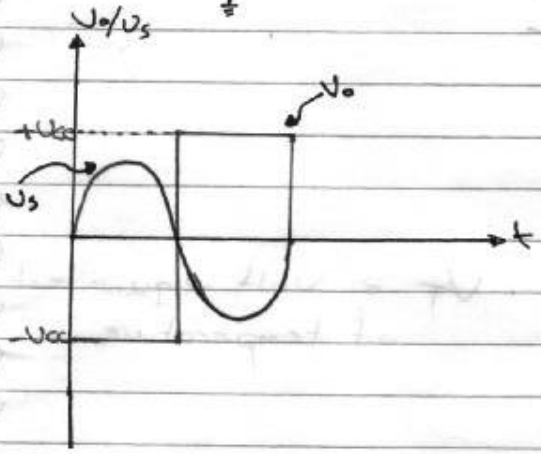
If $V_1 > V_2$

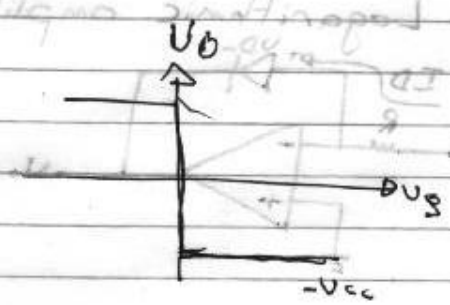
$V_o = -V_{cc}$

If $V_2 > V_1$

$V_o = +V_{cc}$







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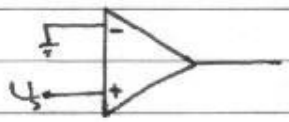
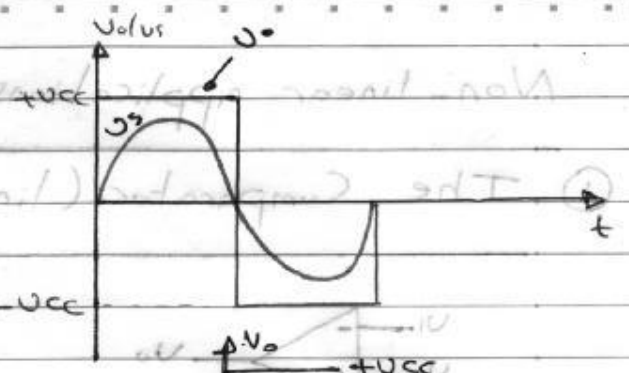
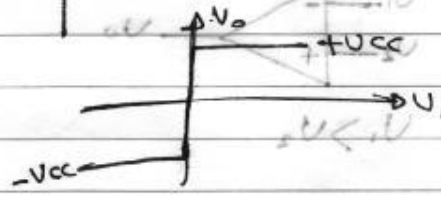
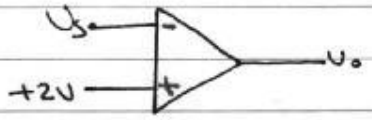
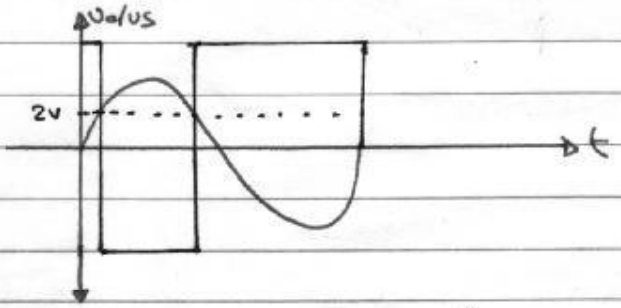






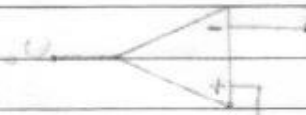
اذا أريد أقارن بغير الـ zero



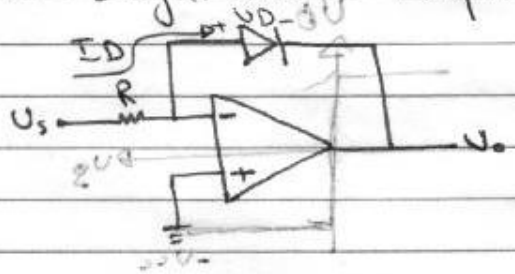


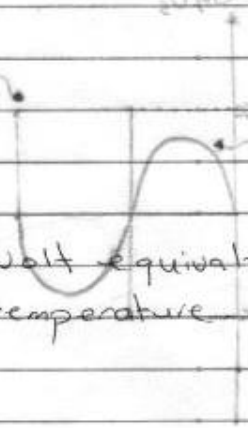
H.W

Transfer e/c's.



2- Logarithmic amplifier:-





V_T = Volt equivalent of temperature

$$I_D = \frac{V_s}{R}$$

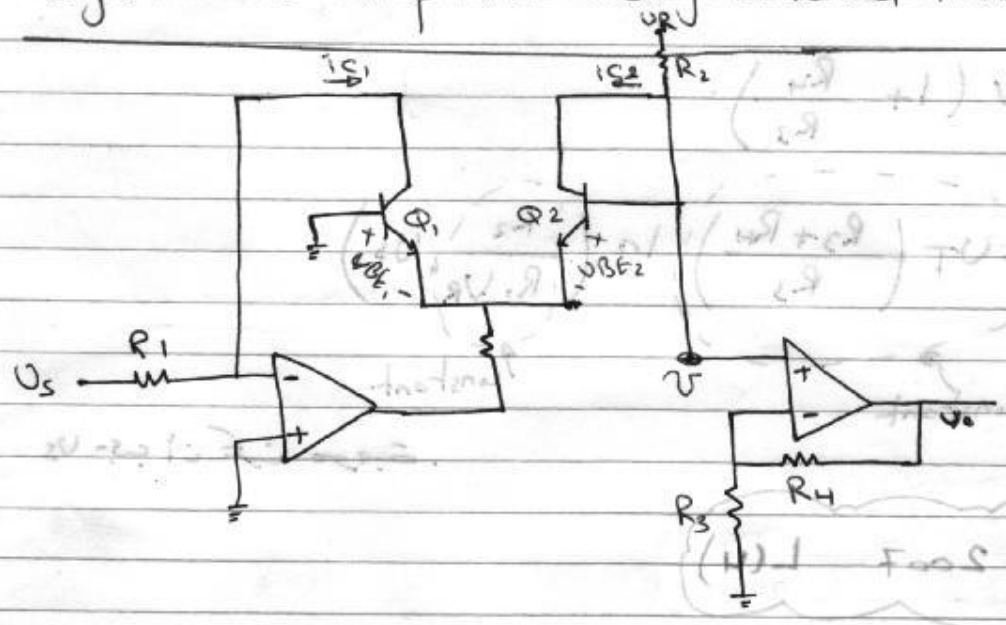
$$V_D = -V_o = V_T \ln \frac{I_D}{I_s}$$

$$V_o = -V_T \ln\left(\frac{V_s}{R I_s}\right)$$

Subject : Date:

$$V_o = -V_T \ln\left(V_S \frac{1}{RI_S}\right)$$

Logarithmic amplifier using matched transistors:-



$$V = V_{BE_2} - V_{BE_1}$$

$$= V_T \ln \frac{i_{C_2}}{I_S} - V_T \ln \frac{i_{C_1}}{I_S}$$

$$= V_T \ln \frac{i_{C_2}}{i_{C_1}}$$

$$= -V_T \ln \frac{i_{C_1}}{i_{C_2}}$$

$i_{C_2} = \frac{V_R}{R_2}$, اذا أهملنا تيار الـ base

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$$iC_1 = \frac{V_S}{R_1}$$

$$V = -V_T \ln\left(\frac{V_S R_2}{R_1 V_R}\right)$$

V_R is a constant.

$$V_o = V\left(1 + \frac{R_4}{R_3}\right)$$

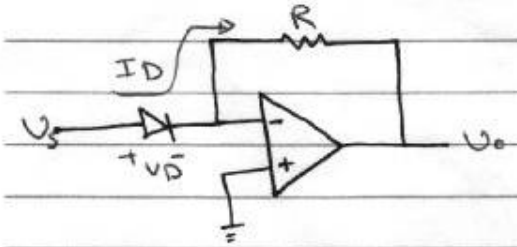
$$V_o = -V_T\left(\frac{R_3 + R_4}{R_3}\right) \ln\left(\frac{R_2}{R_1 V_R} V_S\right)$$

constant

constant.

V_S يجب أن تكون موجبة.

3- Exponential amplifier:-



$$V_D = V_S = V_T \ln \frac{I_D}{I_S}$$

$$I_D = \frac{-V_o}{R}$$

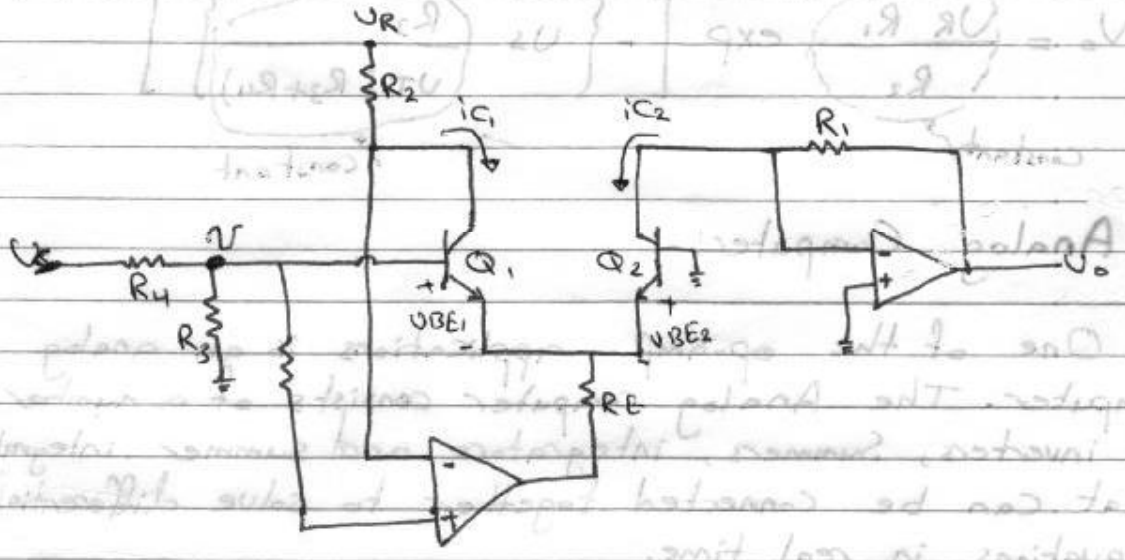
Subject :—— Date:——

$$\frac{V_s}{V_T} = \ln \frac{I_D}{I_S}$$

$$e^{V_s/V_T} = \frac{I_D}{I_S}$$

$$e^{\frac{V_s}{V_T}} = \frac{-V_o}{RI_S} \Rightarrow V_o = -RI_S e^{\frac{V_s}{V_T}}$$

Exponential amplifier (Improved):-



$$V = V_{BE_1} - V_{BE_2}$$

$$= V_T \ln \frac{i_{C_1}}{i_{C_2}}$$

$$i_{C_1} = \frac{V_R}{R_2}$$

$$i_{C_2} = \frac{V_o}{R_1}$$

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$$V = V_T \ln\left(\frac{V_R}{R_2} \cdot \frac{R_1}{V_o}\right)$$

$$V = V_S \frac{R_3}{R_3 + R_4}$$

$$V_S \frac{R_3}{R_3 + R_4} = V_T \ln\left(\frac{V_R R_1}{R_2} \cdot \frac{1}{V_o}\right)$$

$$\exp\left(\frac{V_S}{V_T} \frac{R_3}{(R_3+R_4)}\right) = \frac{V_R R_1}{R_2} \cdot \frac{1}{V_o}$$

$$V_o = \frac{V_R R_1}{R_2} \exp\left[-\left\{V_S \frac{R_3}{V_T (R_3+R_4)}\right\}\right]$$

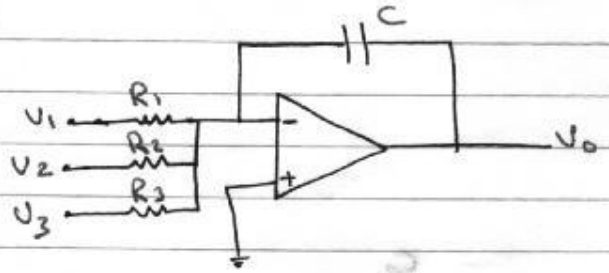
Constant — Constant

Analog Computer:-

One of the op-amp applications is an analog computer. The Analog computer consists of a number of inverters, Summers, integrators and summer-integrator that can be connected together to solve differential equations in real time.

Subject : Date:

The Summer integrator unit:-



$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = -C\frac{dV_o}{dt}$$

$$V_o = -\int\left[\frac{V_1}{CR_1} + \frac{V_2}{CR_2} + \frac{V_3}{CR_3}\right]dt$$

Example:-

Solve the following differential equation using an analog computer :-

$$\frac{V_o}{3} + 2\frac{dV_o}{dt} + \frac{d^2V_o}{dt^2} = V_m \cos\omega t \quad , \quad \left.\frac{dV_o}{dt}\right|_{t=0} = -1V$$

Solution:-

$$\frac{d^2V_o}{dt^2} = -2\frac{dV_o}{dt} - \frac{V_o}{3} + V_m \cos\omega t$$

$$\frac{dV_o}{dt} = \int_0^t \frac{d^2V_o}{d\lambda^2}\,d\lambda$$

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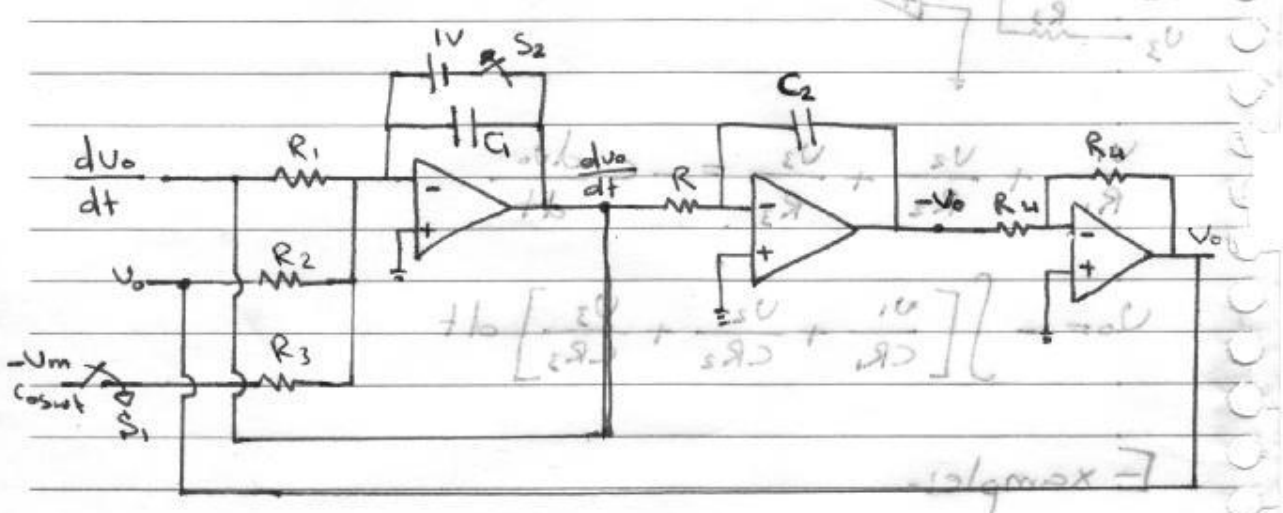
$$\frac{dv_o}{dt} = \int_0^t \left(-2\frac{dv_o}{d\lambda} - \frac{v_o}{3} + v_m \cos\omega\lambda \right) d\lambda$$

$$v_o = \int_0^t \frac{dv_o}{d\lambda}\, d\lambda$$



Initially S_1 is opened and S_2 is closed, then close S_1 and open S_2 simultaneously to start operation.

$$\frac{1}{R_1 C_1} = 2$$

$$\frac{1}{R_2 C_1} = \frac{1}{3} \quad \text{if } C_1 = 1\mu F$$

$$\frac{1}{R_3 C_1} = 1 \qquad \therefore R_1 = 0.5\,M\Omega$$

$$R_2 = 3\,M\Omega$$

$$R_3 = 1\,M\Omega$$

$$\frac{1}{RC_2} = 1 \quad \text{if } C_2 = 1\mu F \text{ \& } R = 1M\Omega$$

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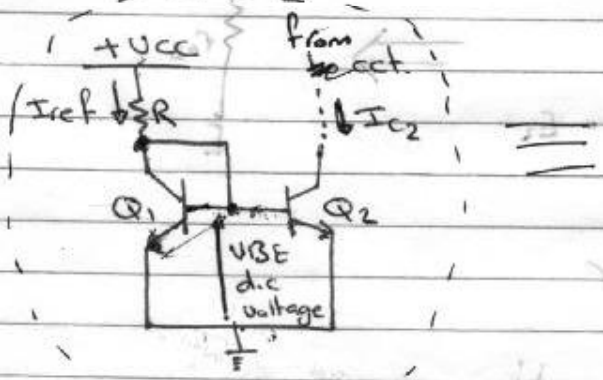
$\frac{R_4}{R_4} = 1$

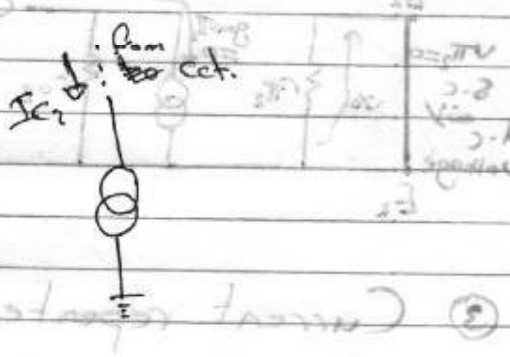
$R_4 = 1M\Omega$

IC Biasing Techniques:-

Biasing in IC's is accomplished through the use of constant current sources which are comprised mainly of transistors so that they occupy a small area compared to large resistors.

① Constant current (sink)





sink ⇒ npn

$I_{C_2} = \frac{I_{ref}}{1 + \frac{2}{\beta}}$, $I_{ref} = \frac{V_{cc} - 0.7}{R}$

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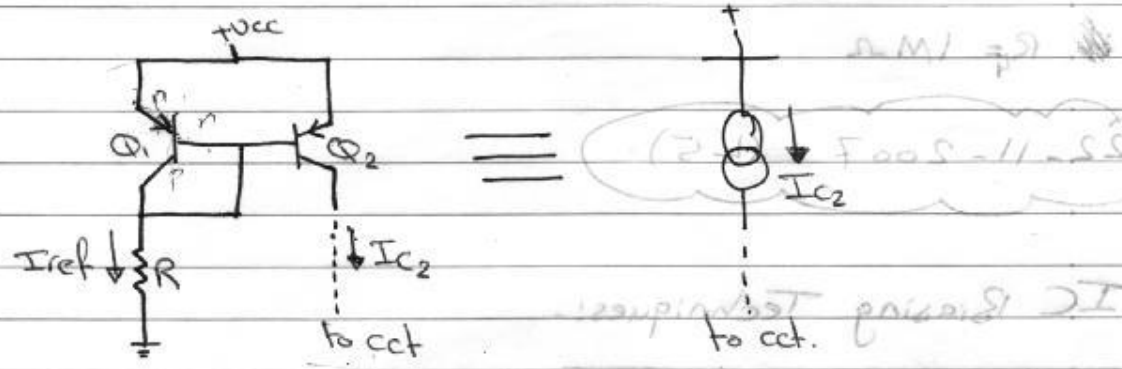
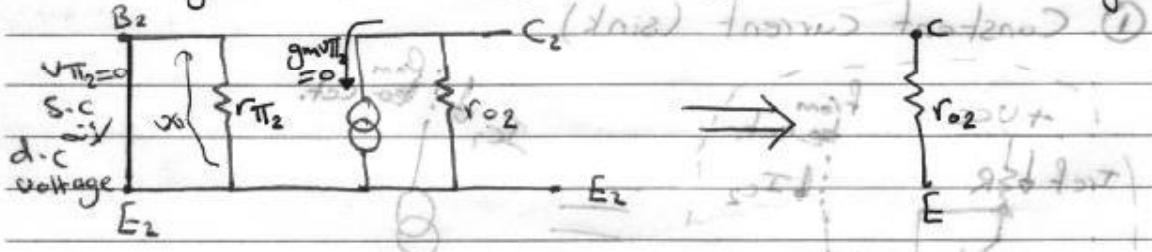
② Constant current source

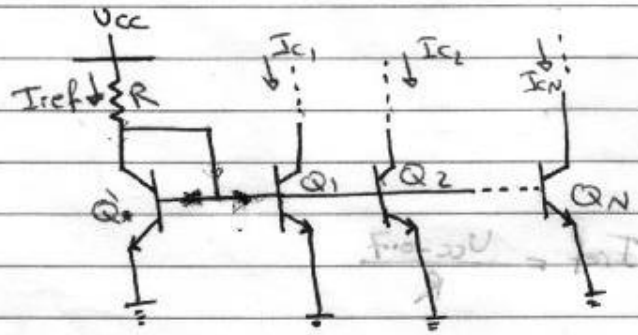


source يعني pnp

for both current source (source and sink) the a.c small signal BJT model for Q_2 is the following:-



③ Current repeater



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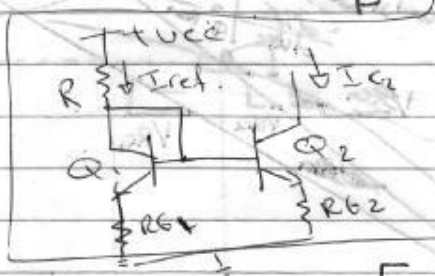
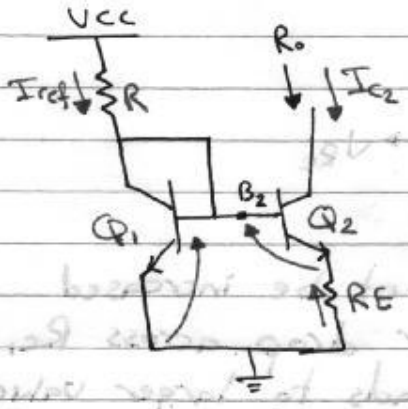
$$I_{C_1} = I_{C_2} = \cdots = I_{CN} = \frac{I_{ref}}{1 + \frac{(N+1)}{\beta}}$$

(4) Ratio Constant Current Source

$$\frac{I_{C_2}}{I_{ref}} = \frac{R_{E_1}}{R_{E_2}}$$



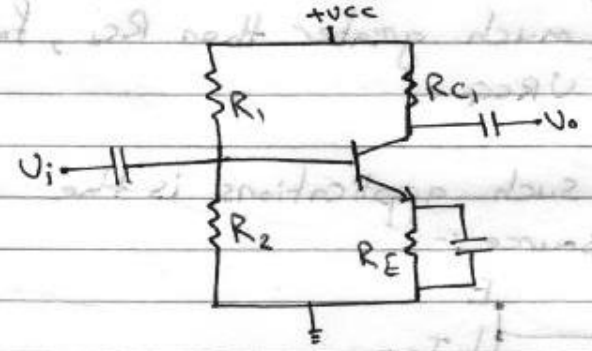
(5) Widlar CCS



$$R_{occs} = r_{o_2}\left[1 + \frac{\beta_o R_E}{r_{\pi_2} + R_E}\right]$$

$$I_{C_2} R_E = V_T \ln \frac{I_{ref}}{I_{C_2}}$$

Active and non-linear loads in BJT amplifiers:-



$$A_V = \frac{V_o}{V_i} = \frac{-g_m V_\pi R_{C_1}}{V_\pi} = -g_m R_{C_1} \quad (\text{if } R_s = 0,\ r_o \to \infty)$$

More precisely:-

$$A_V = -g_m (R_{C_1} \| r_o)$$

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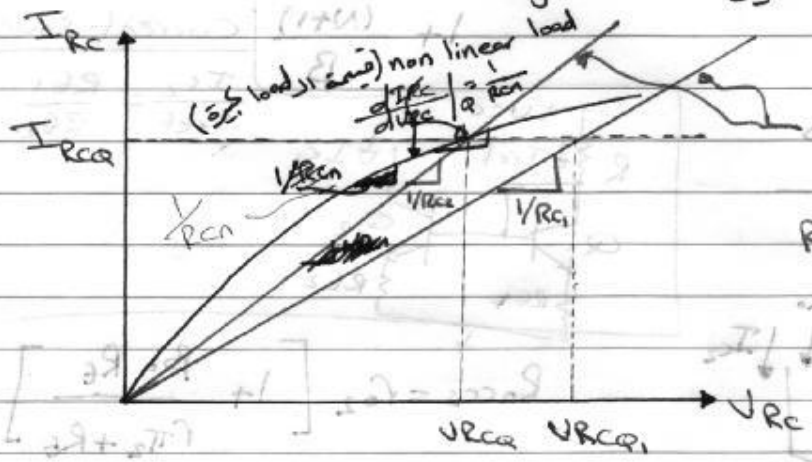
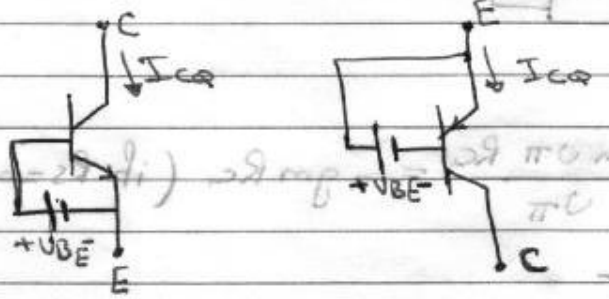
* كلما كبر الـ R_{c_1} يزداد الـ a.c gain.



To increase the gain R_{c_1} must be increased which leads to a greater drop across R_{c_1} for the same I_{CQ}, this leads to larger values of V_{CC} which are not practical for an IC. To solve the problem, a non-linear load is used whose value R_{cn} is much greater than R_{c_1}, for the same I_{RCQ} and V_{RCQ}.

An ideal device for such applications is the transistor current source :-



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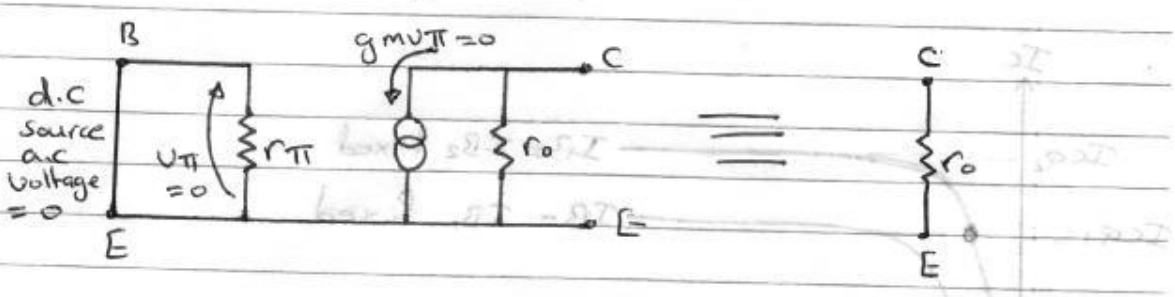
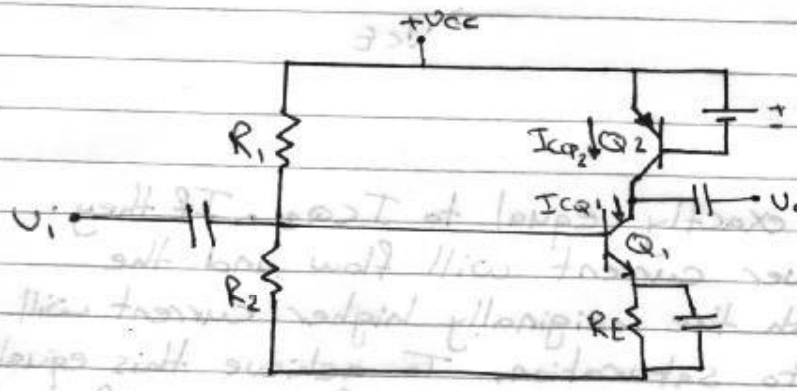
active load equi cct. :=



and the circuit becomes



active load الـ Q1 هو npn اذاً يجب أن يكون الـ [redacted] (pnp).

ICQ1 bias established from T1.
ICQ2 bias established from T2.

* يجب ان يكون ICQ1 = ICQ2

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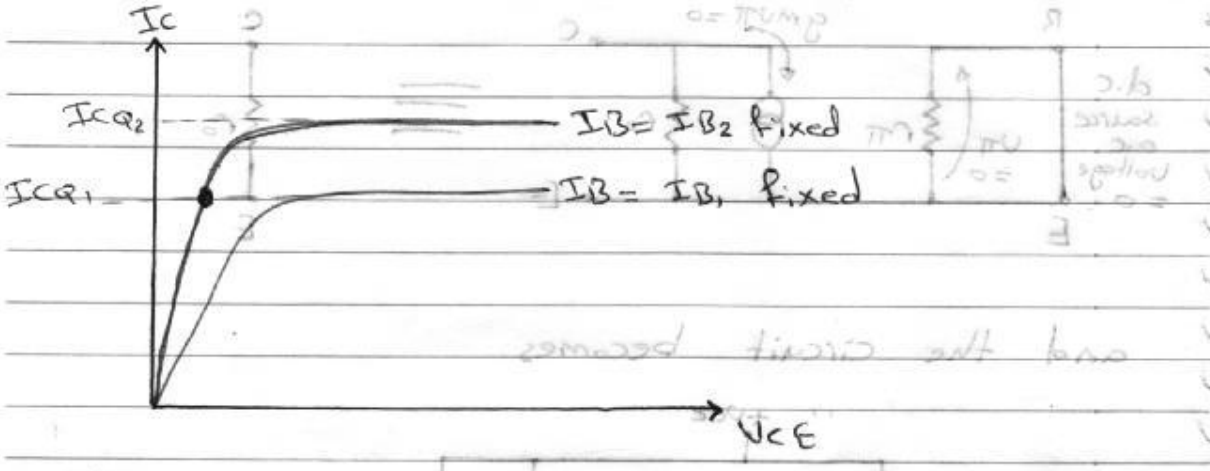
assume $I_{CQ_2} > I_{CQ_1}$.



note:-

I_{CQ_1} must be exactly equal to I_{CQ_2}. If they differ, the lower current will flow and the transistor with the originally higher current will be drawn into saturation. To achieve this equality we duplicate the biase circuit of the amplifier and use the duplicate to biase the ccs (active load) via a current mirror.

We do so because, for an IC, we may comfortably assume that devices and components of the same shape and size will have the same characteristics.

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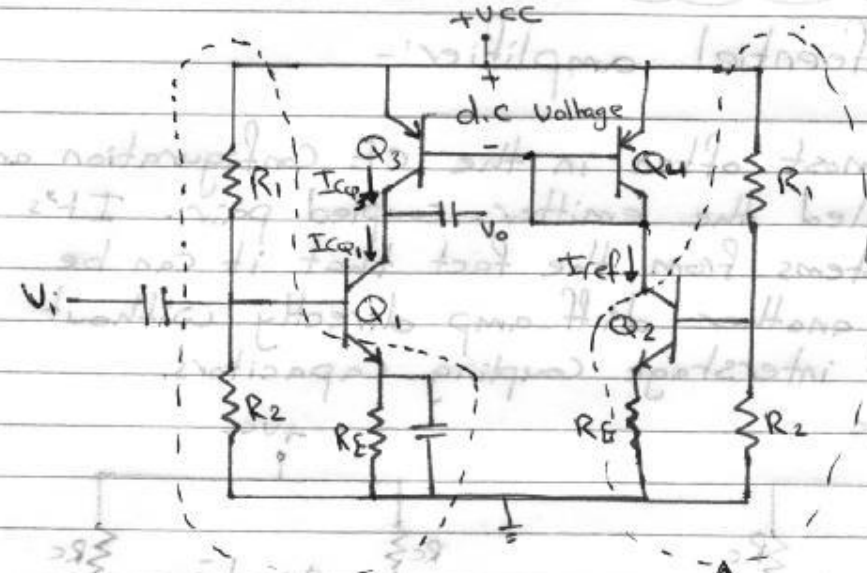


the duplicated bias circuit.

Q_1 and Q_2 are prefectly matched.

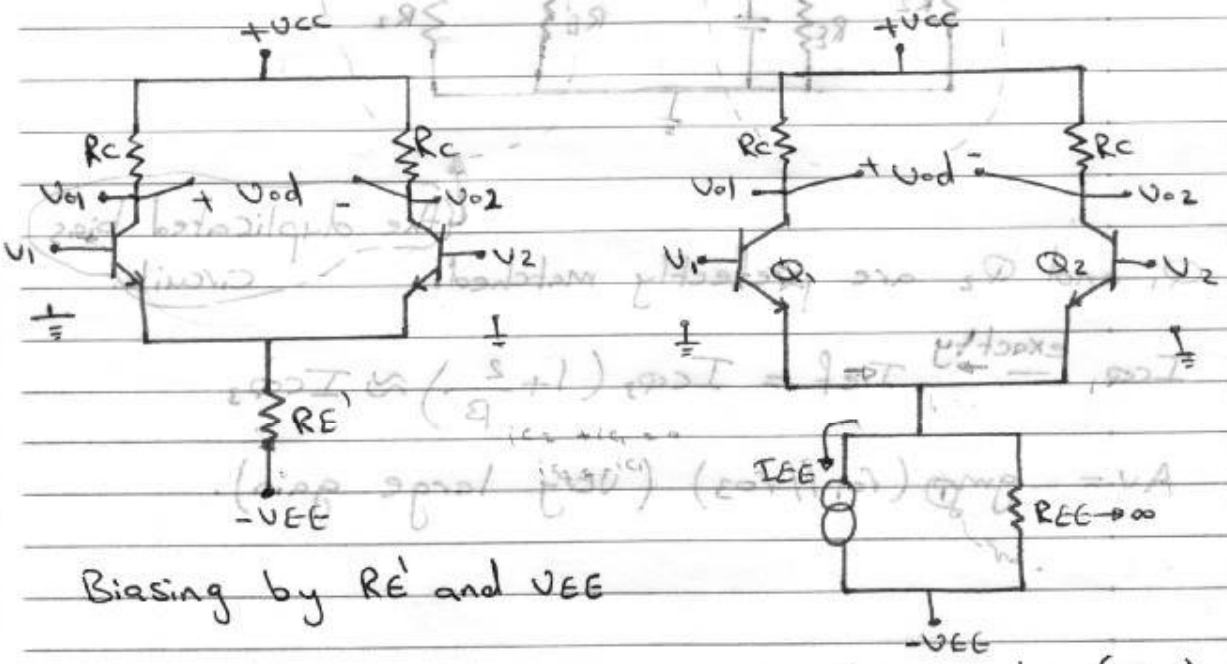
$I_{CQ_1} \overset{\text{exactly}}{=} I_{ref} = I_{CQ_3}\left(1+\frac{2}{\beta}\right) \approx I_{CQ_3}$

$A_V = -g_{m_{Q_1}}(r_{o_1} \,//\, r_{o_3})$ (very large gain).

Date:

The differential amplifier:-

This is most often in the CE configuration and is thus called the emitter-coupled pair. It's usefulness stems from the fact that it can be coupled to another diff-amp directly without the use of interstage coupling capacitors.



Vo1 and Vo2 :- single ended outputs.

Vod :- differential outputs.

Vod = Vo1 − Vo2.

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when $v_1 = v_2$

for the 1'st cct:-

v_{o1} a.c and v_{o2} a.c exist but $v_{od} = 0$

for the 2'nd circuit (CCS):-

v_{o1} a.c $= 0$ and v_{o2} a.c $= 0$ and $v_{od} = 0$

when $v_1 = -v_2$

$v_1 - v_2 = 2v_1$

$\therefore v_{od} = 2v_{o1}$

As difference increases, v_{od} increases. Therefore the diff-amp amplifies the difference between the two inputs.

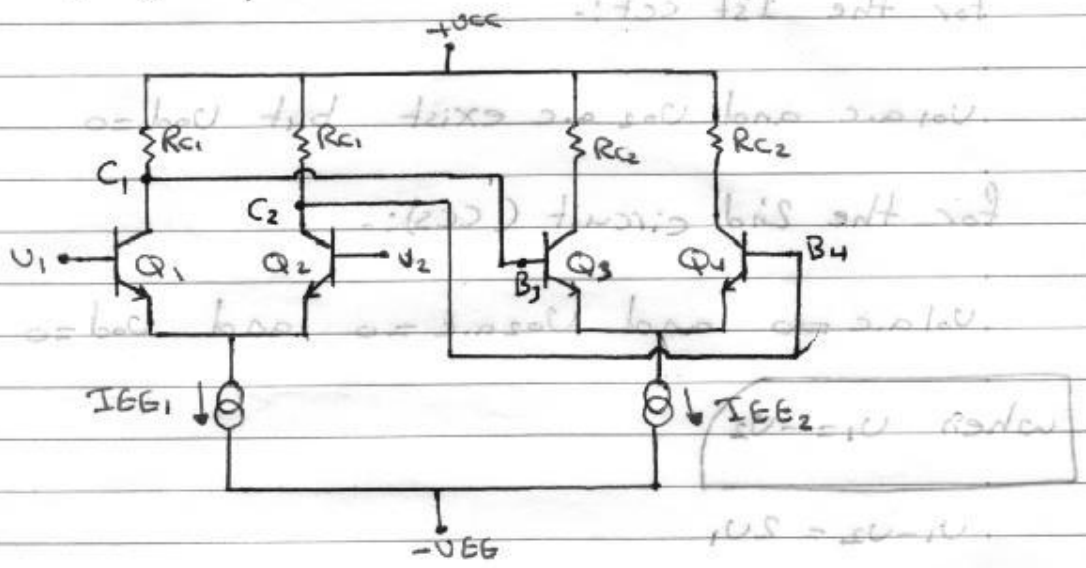
$v_1 = v_2$ results in the so-called pure common-mode (CM) input signal. $V_1 = -V_2$ results in a pure difference-mode (DM) input.

Otherwise, the input consists of both a CM and a DM component.

If two diff-amps with ideal CCSs are cascaded, the d.c outputs of the 1st stage will constitute a CM signal at the input of the second stage. Therefore, these d.c:

Subject : Date:

outputs will not be amplified because 2nd stage employes an ideal CCS thereby eliminating the need for coupling capacitance.



$V_{1d.c} = V_{2d.c} = 0$

$V_{B_3 d.c} = V_{C_1 d.c}$

$V_{B_4 d.c} = V_{C_2 d.c}$

$V_{C_1 d.c} = V_{C_2 d.c}$

$V_{B_3 d.c} = V_{B_4 d.c}$

$V_{C_3 d.c}$ and $V_{C_4 d.c}$ will not be effected by the d.c voltage at B_3 and B_4.

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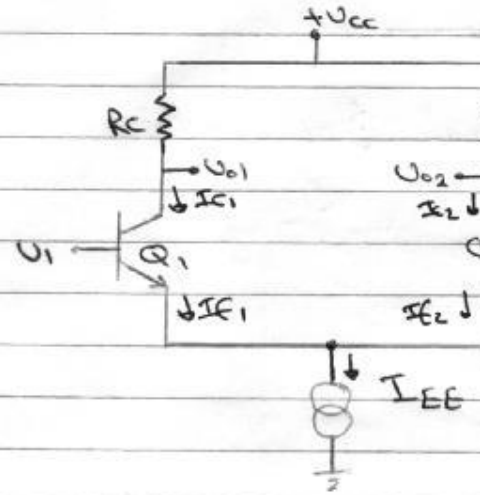
D.C transfer characteristics



$V_1 - V_{BE_1} + V_{BE_2} - V_2 = 0$

$V_1 - V_2 = V_{BE_1} - V_{BE_2} = V_{id}$

$I_{C_1} = I_S e^{V_{BE_1}/V_T}$

$V_{BE_1} = V_T \ln \frac{I_{C_1}}{I_{S_1}}$

$V_{BE_2} = V_T \ln \frac{I_{C_2}}{I_{S_2}}$

$V_{BE_1} - V_{BE_2} = V_T \ln \frac{I_{C_1}}{I_{C_2}}$

$I_{S_1} = I_{S_2}$ (due to perfect symmetry).

$V_{id} = V_T \ln \frac{I_{C_1}}{I_{C_2}}$

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$$\frac{I_{C1}}{I_{C2}} = e^{V_{id}/V_T}$$

$I_{E1} + I_{E2} = I_{EE}$

$\alpha I_{EE} = I_{C1} + I_{C2}$, $I_C = \alpha I_E$

$$\frac{\alpha I_{EE}}{I_{C1}} = 1 + \frac{I_{C2}}{I_{C1}}$$

$$\frac{\alpha I_{EE}}{I_{C1}} = 1 + e^{-V_{id}/V_T}$$

$$I_{C1} = \frac{\alpha I_{EE}}{1 + e^{-V_{id}/V_T}}$$

Similarly:-

$$I_{C2} = \frac{\alpha I_{EE}}{1 + e^{V_{id}/V_T}}$$

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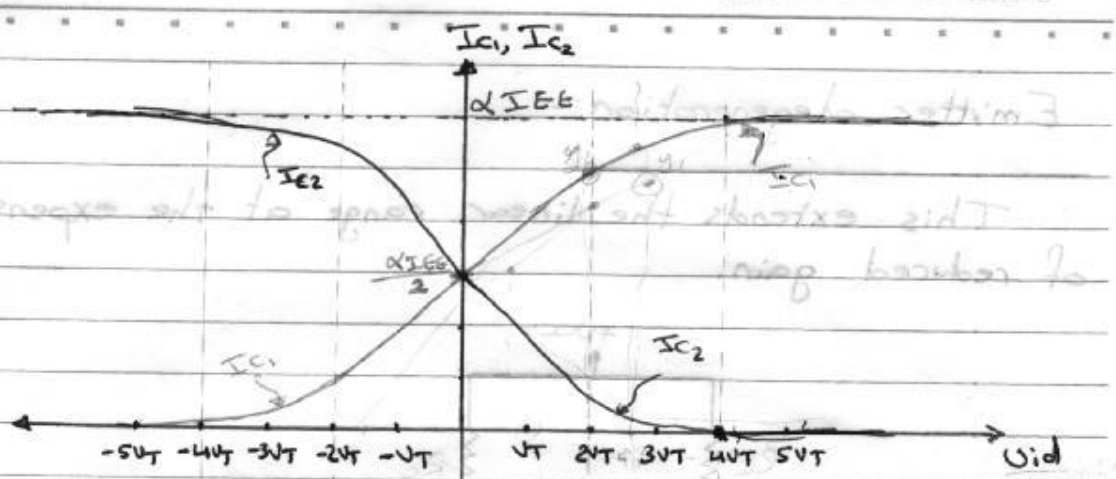


linear region

$\mp 2V_T = \pm 50mV$

non-linear or switching region.

non-linear or switching region

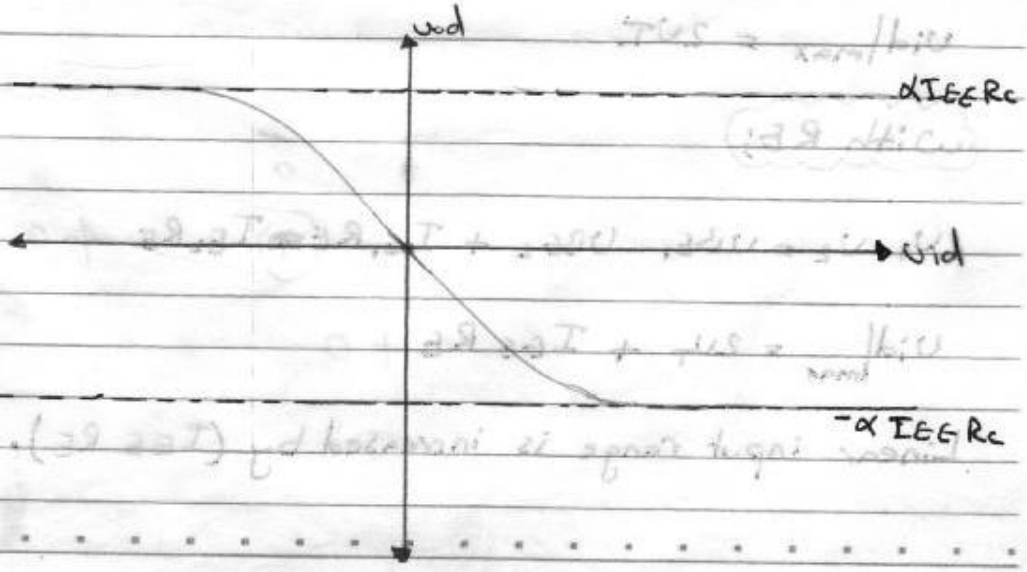
$V_{o1} = V_{cc} - I_{C1} R_c$

$V_{o2} = V_{cc} - I_{C2} R_c$

$V_{od} = V_{o1} - V_{o2}$

$= (-I_{C1} + I_{C2}) R_c$

$= \alpha I_{EE} R_c \tanh\left(\frac{-v_{id}}{2V_T}\right)$



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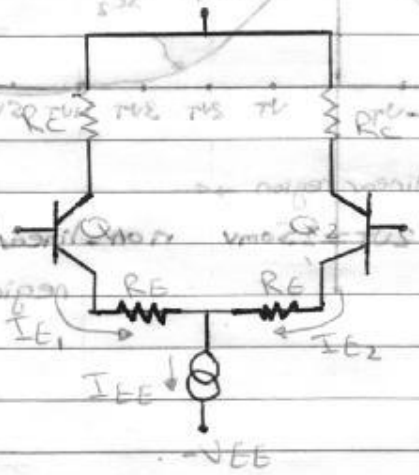
Emitter degeneration

This extends the linear range at the expense of reduced gain.



Without RE;

$V_1 - V_2 = V_{BE1} - V_{BE2}$

$v_{id} = V_{BE1} - V_{BE2}$

$v_{id}|_{max} = 2V_T$

With RE;

$V_1 - V_2 = V_{BE1} - V_{BE2} + I_{E1}R_E - I_{E2}R_E$

$v_{id}|_{max} = 2V_T + I_{EE}R_E$

Linear input range is increased by $(I_{EE}R_E)$.

Subject :- Date:-

a.c analysis:-

we assume that V_1 and V_2 are small enough so that they do not violate the assumption of linear operation.

$V_a = \underset{\text{average}}{\frac{V_1 + V_2}{2}}$ CM input signal

$V_d = \underset{\text{difference}}{V_1 - V_2}$ DM input signal.

Solving the above two equations for V_1 and V_2:-

$$V_1 = \frac{V_d}{2} + V_a$$

$$V_2 = \frac{-V_d}{2} + V_a$$

Similarly:-

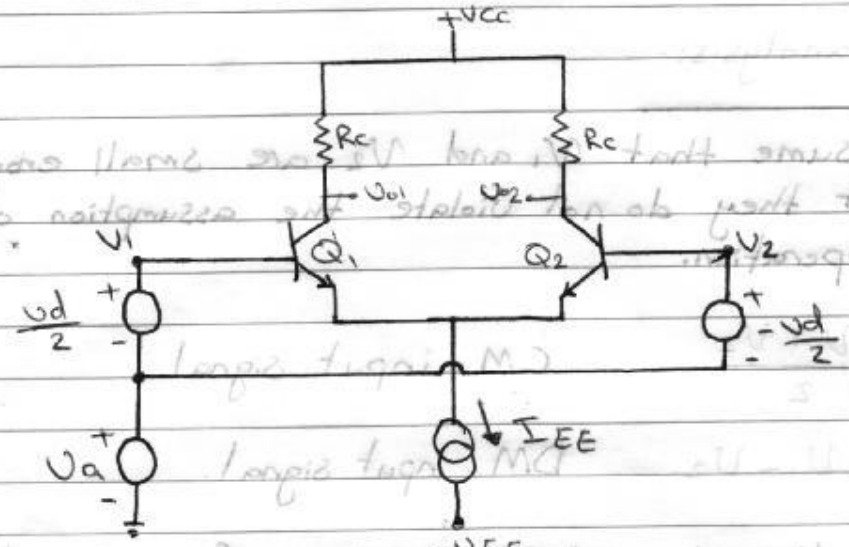
$V_{oa} = \frac{V_{o1} + V_{o2}}{2}$ CM o/p

$V_{od} = V_{o1} - V_{o2}$ DM o/p

$$\therefore V_{o1} = \frac{V_{od}}{2} + V_{oa}$$

$$V_{o2} = \frac{-V_{od}}{2} + V_{oa}$$

Subject : Date:



Define the DM gain as Ad

$$Ad = \frac{Vod/2}{Vd}$$

and the CM gain as Ac

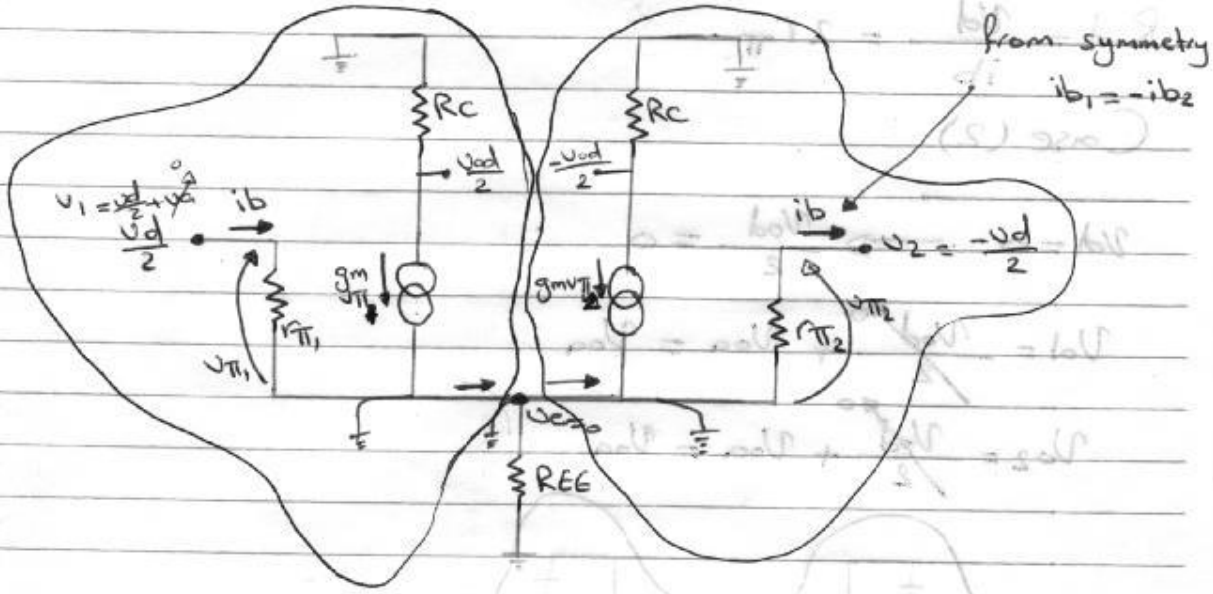
$$Ac = \frac{Voa}{Va}$$

Ad and Ac are single ended gains.

Subject : Date:

Half Circuit Concept:-

Case 1:- $V_a = 0 \longrightarrow V_{oa} = 0$



$V_c = 0$ due to exact symmetry and the fact that $V_1 = -V_2$.

Thus we may use the half circuit concept:-

$$\frac{V_{od}}{2} = -g_m V_{\pi_1} R_c$$

$$V_{\pi_1} = \frac{V_d}{2}$$

$$\therefore \frac{V_{od}}{2} = -g_m \frac{V_d}{2} R_c$$

$$A_d = \frac{V_{od}/2}{V_d} = \frac{-g_m R_c}{2}$$

$$\boxed{A_d = \frac{-g_m R_c}{2}}$$

Subject : Date:

R_{id} :- differential input resistance, resistance seen by the two bases.

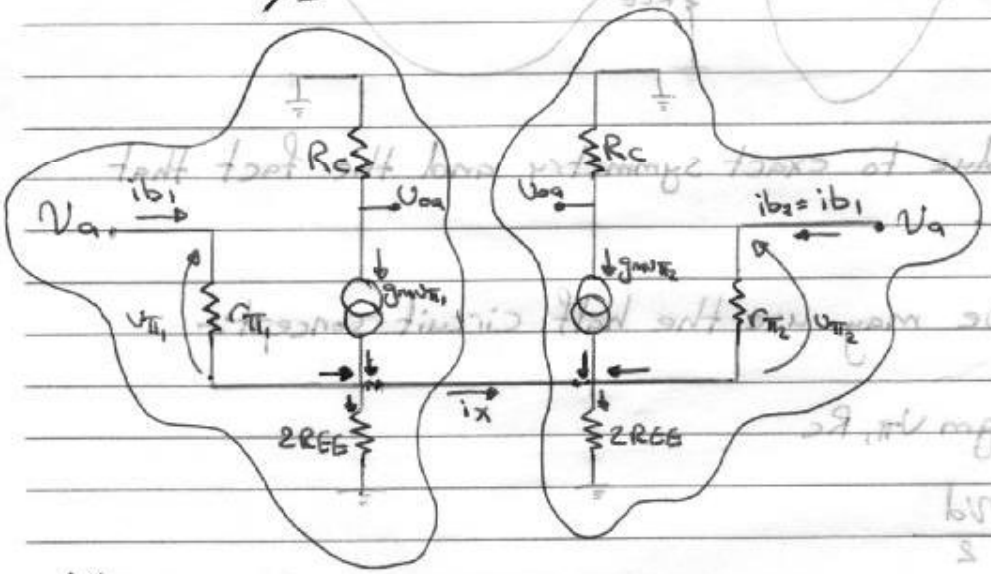
$$R_{id} = \frac{v_d}{i_b} = 2r_\pi .$$

Case (2)

$$v_d = 0 \Longrightarrow \frac{v_{od}}{2} = 0$$

$$v_{o1} = \frac{v_{od}}{2}^{0} + v_{oa} = v_{oa}$$

$$v_{o2} = \frac{v_{od}}{2}^{0} + v_{oa} = v_{oa}$$



$i_X = 0$

Subject : Date:

A_c = CM gain

$$A_c = \frac{v_{oa}}{v_a}$$

Using one half of the ckt.

$$v_{oa} = -g_m v_{\pi_1} R_c$$

$$= -g_m R_c (i_{b_1} r_{\pi_1}), \quad r_{\pi_1} = r_{\pi_2} = r_\pi$$

$$= \frac{-\beta_o R_c v_a}{r_\pi + 2R_{EE}(1+\beta_o)}$$

$$A_c = \frac{-\beta_o R_c}{r_\pi + 2R_{EE}\beta_o\left(1+\frac{1}{\beta_o}\right)}, \quad \beta_o = g_m r_\pi$$

$$\boxed{A_c = \frac{-g_m R_c}{1 + 2 g_m R_{EE}\left(1+\frac{1}{\beta_o}\right)}}$$

for an ideal CCS, $R_{EE} \to \infty$

$A_c \to 0$

Subject : Date:

R_{ic} :- Common mode i/p resistance

$$R_{ic} = \frac{V_a}{i_b}$$

$$R_{ic} = r_\pi + 2R_{EE}(1+\beta_o)$$

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CMRR : Common-Mode Rejection Ratio.

$$CMRR = \left| \frac{A_{dl}}{A_c} \right|$$

CMRR must be as large as possible.

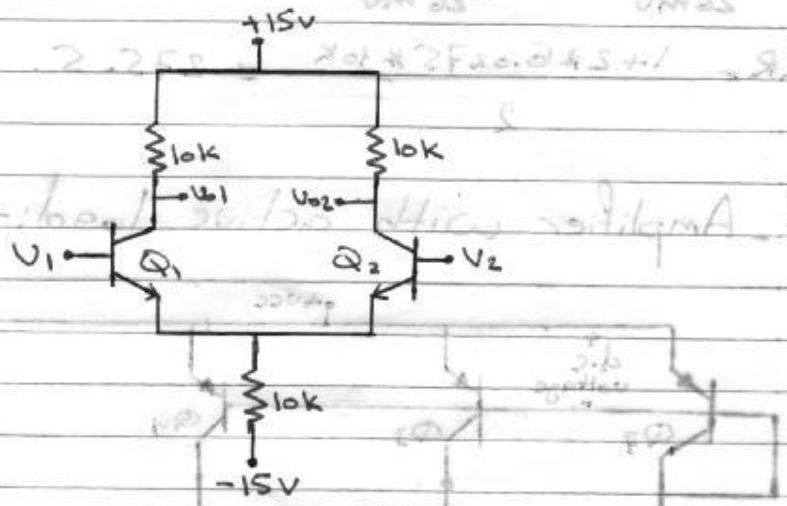
$$CMRR = \frac{1 + 2 g_m R_{EE}\left(1 + \frac{1}{\beta_o}\right)}{2}$$

For an ideal ccs, $R_{EE} \to \infty$
$A_c \to 0$, $CMRR \to \infty$

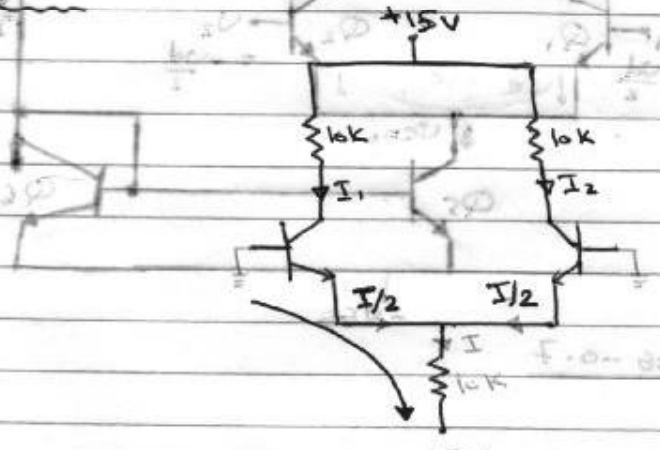
Subject : Date:

Example:-

Calculate CMRR for the given circuit. (Both)



Solution:-



$0 - 0.7 - I * 10k + 15 = 0$

$I = \frac{15 - 0.7}{10k}$, $I = 1.43$ mA.

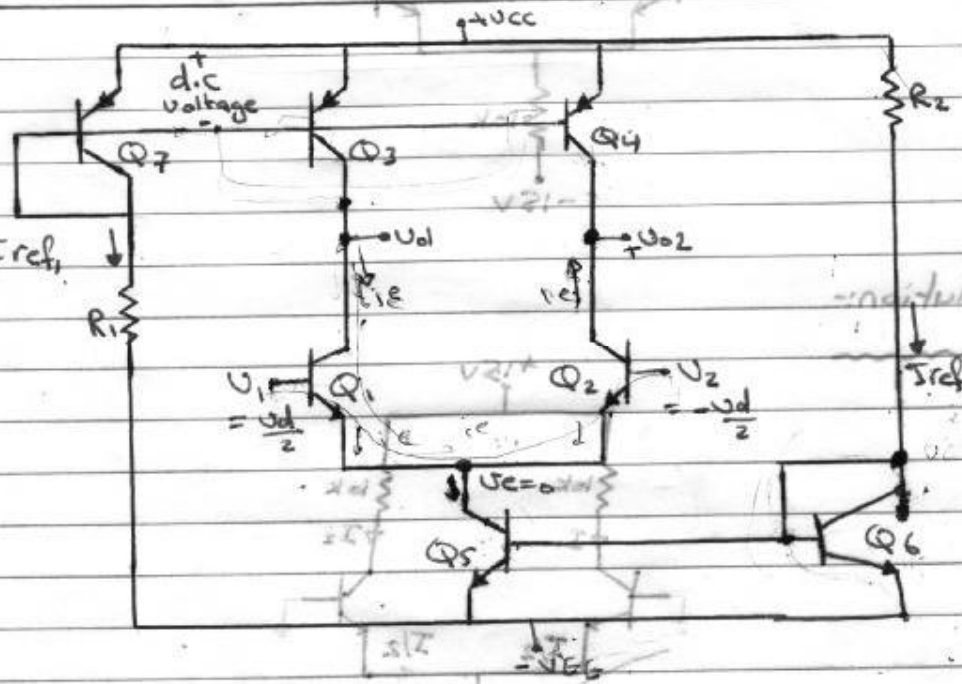
Subject : Date:

$$I_1 = I_2 = I/2 = \frac{1.43}{2} = 0.715 \text{ mA}.$$

$$g_m = \frac{|I_{CQ1}|}{26mV} = \frac{0.715mA}{26mV} = 0.0275 \frac{1}{\Omega}$$

$$CMRR = \frac{1+2*0.0275*10K}{2} = 275.5.$$

Diff. Amplifier with active load:-



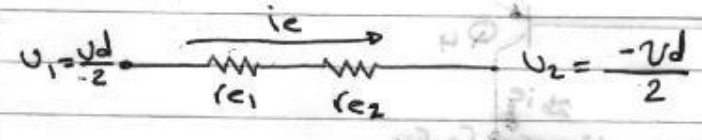
$$I_{ref} = \frac{V_{CC} + V_{EE} - 0.7}{R}$$

$$I_{ref1} = \frac{1}{2} I_{ref2}.$$

$$\therefore R_1 = 2R_2.$$

Subject: Date:

$$\frac{V_{o2}}{V_d} = -A_d = \frac{-V_{o1}}{V_d} \quad \text{(single ended gain).}$$



$$r_{e1} = r_{e2} = r_e \;, \quad r_e = \frac{V_T}{|I_{EQ}|}$$

$$i_e = \frac{\frac{v_d}{2} - \left(\frac{-v_d}{2}\right)}{2r_e} = \frac{v_d}{2r_e}$$

$$\frac{1}{r_e} \approx g_m \;, \quad i_e = \frac{g_m v_d}{2}$$

$$V_{o2} = i_e (r_{o4} \| r_{o2})$$

$$= + \frac{g_m v_d}{2} (r_{o4} \| r_{o2})$$

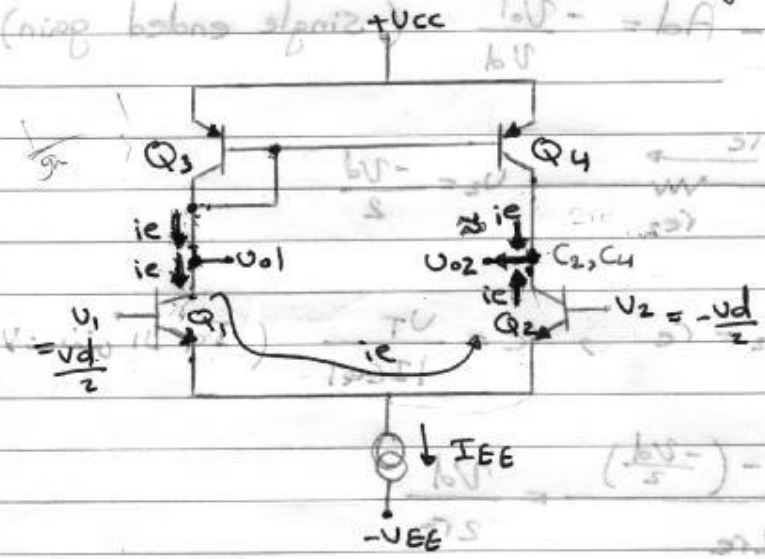
$$\boxed{\frac{V_{o2}}{V_d} = + \frac{g_m}{2} (r_{o4} \| r_{o2})}$$

$$A_d = \frac{V_{o1}}{V_d} = - \frac{g_m}{2} (r_{o1} \| r_{o3}).$$

$$r_{o1} = r_{o2} \;, \; r_{o3} = r_{o4}$$

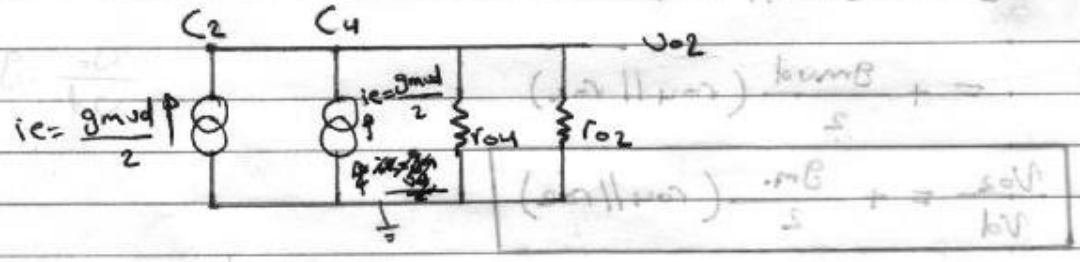
Subject : Date:

Another Circuit with twice the single-ended gain of the 1st cct. is the following :-



Current mirror active load

$$ie = \frac{g_m v_d}{2}$$



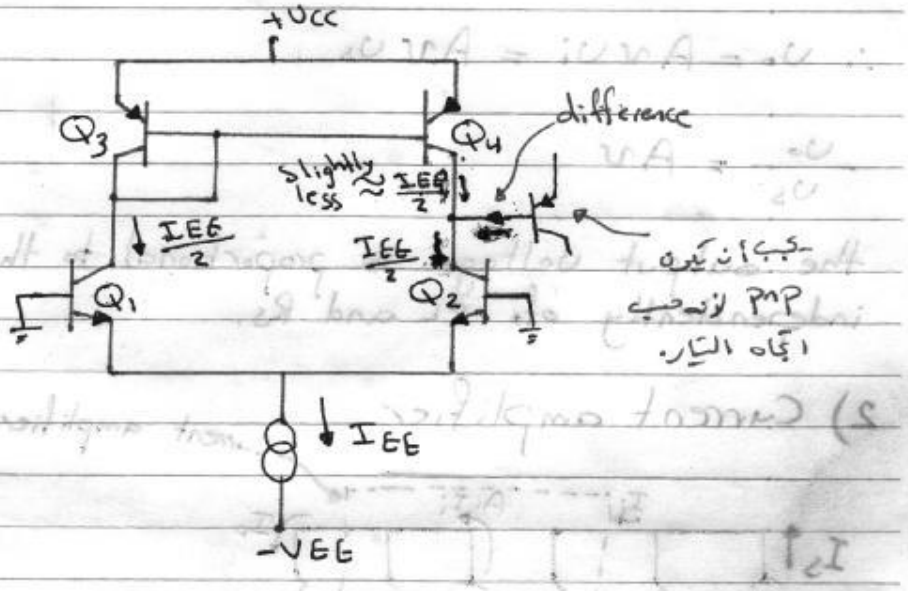
$$V_{o2} = + g_m v_d (r_{o4} \parallel r_{o2})$$

$$\frac{V_{o2}}{V_d} = + g_m (r_{o2} \parallel r_{o4})$$ twice gain of previous circuit.

$\frac{V_{o1}}{V_d}$ is comparitively negligible.

Subject : Date:

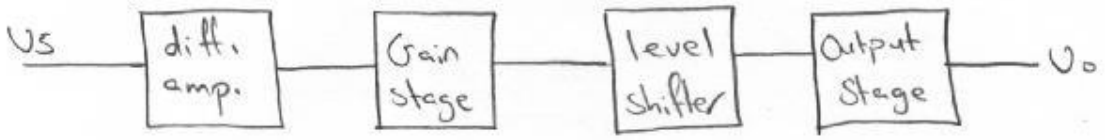
The d.c currents and voltages in such a differential amplifier are as following:-



Operational Amplifier Specifications:-

(1) Offset voltages and input bias current:-

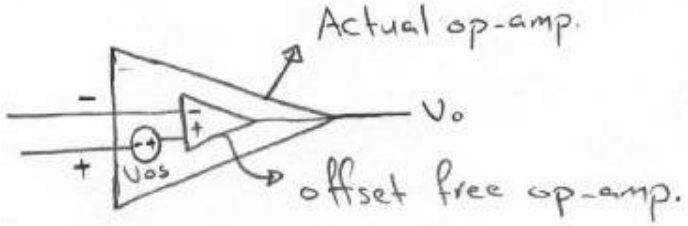
(a) Offset voltage



Block diagram of the op-amp.

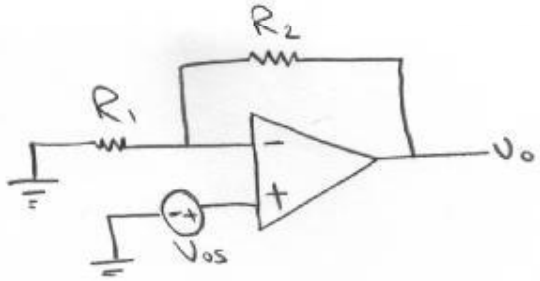
Mismatches between input devices of the diff-amp. stage may create an output voltage with zero input, this voltage is called the output offset voltage (V_{os}) for an open looped op-amp.

V_{os} has a typical value of (1-5mv)



cct. model for an op-amp. with input offset voltage

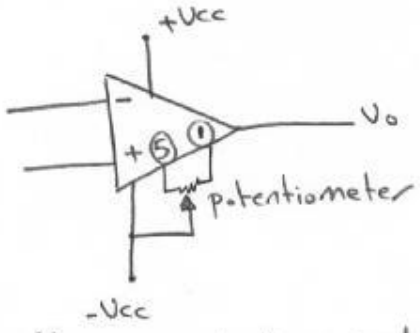
To find the effect of the offset voltage :- the input voltage signal source is short circuited. Following this procedure, we get the cct. shown below (for the inverting and non-inverting op-amp. configuration):-



$$V_o = \left(1 + \frac{R_2}{R_1}\right) V_{os}$$

Offset Voltage Compensation:-

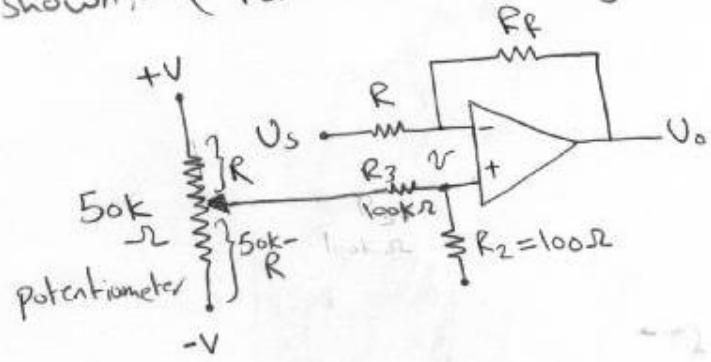
(a) An op-amp. with offset-null terminals:-



(1) and (5) are offset-null terminals.

(b) An externally connected offset compensation network

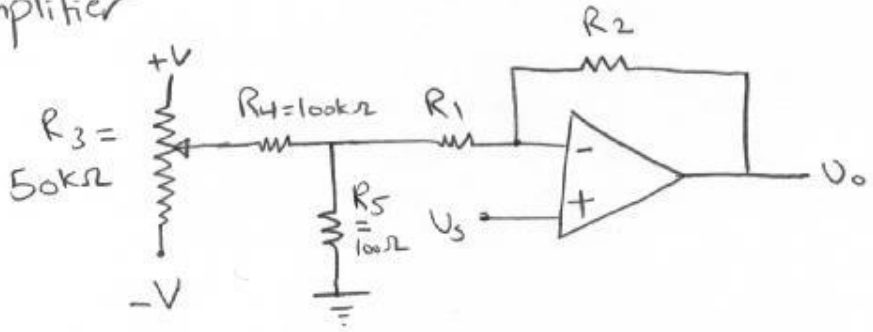
Another method is by applying a small DC voltage at the input so as to cause the D.C output voltage to become Zero as shown:- (For the inverting op-amp.)



$$-15\frac{R_2}{R_3+R_2} < v < +15\frac{R_2}{R_3+R_2} \quad \text{if} \quad V=15V.$$

$$-15mV < v < +15mV$$

Offset voltage Compensation for the non-inverting amplifier



(b) Input Bias Currents

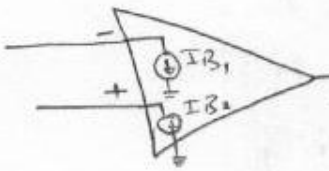
The input bias currents are usually specified by their average value (I_B) which is called the input bias current:-

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

and by their difference which is called the input offset current, and is given by:-

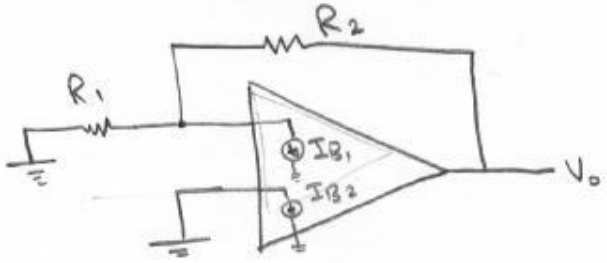
$$I_{os} = |I_{B1} - I_{B2}|$$

* Typical values for op-amps using BJTs are $I_B = 100nA$, and $I_{os} = 10nA$.
* For an op-amp. using FETs (in the order of picoamperes).



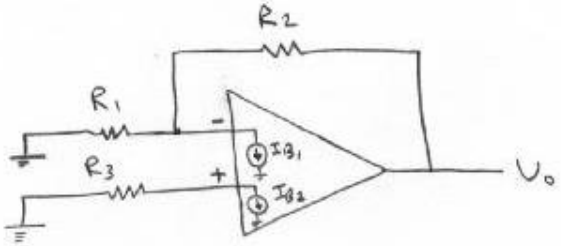
The op-amp. input bias currents represented by

To see the effect of the biasing currents on the operation of the op-amp. To do this, the signal source is grounded and we obtain the cct. shown below :- (for the inverting and non-inverting op-amp).



$$V_o = I_{B_1} R_2 \approx I_B R_2 .$$

The effect of the biasing currents on the o/p D.C voltage can be reduced using a simple compensation technique. This compensation technique is done by adding a resistor (R_3) in series with the non-inverting input terminal as shown:-



$$V_o = I_{B_1} R_2 - I_{B_2} R_3 R_2 \left(\frac{R_1 + R_2}{R_1 R_2} \right)$$

$$I_{B_1} = I_B + \frac{I_{os}}{2}$$

$$I_{B_2} = I_B - \frac{I_{os}}{2}$$

$$V_o(\text{due to } I_B) = R_2 I_B - I_B R_3 R_2 \left(\frac{R_1 + R_2}{R_1 R_2} \right)$$

if $R_3 = R_1 \parallel R_2$

V_o (due to I_B) = Zero

V_o (due to I_{os}) $= R_2 \frac{I_{os}}{2} + \frac{I_{os}}{2} R_3 R_2 \left(\frac{R_1+R_2}{R_1 R_2}\right)$

if $R_3 = R_1 \parallel R_2$

then V_o (due to I_{os}) $= I_{os} R_2$

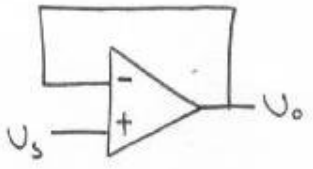
V_o (offset voltage + biasing currents) $= I_{os} R_2 + V_{os}\left(1 + \frac{R_2}{R_1}\right)$.

(2) Slew Rate:-

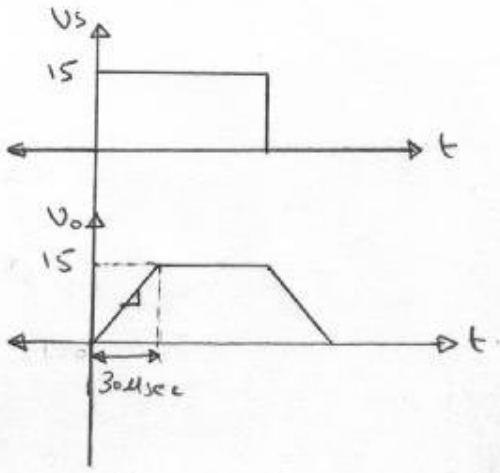
The slew rate is the maximum rate at which the o/p changes with time.

$$SR = \left.\frac{dV_o}{dt}\right|_{max.}$$

Example:-



SR = 0.5 V/μsec.



if $V_s = V_m \sin \omega t$, is applied to a voltage follower.

$V_o = V_m \sin \omega t$

$$\frac{dV_o}{dt} = V_m \omega \cos \omega t$$

$$\left.\frac{dV_o}{dt}\right|_{max} = V_m \omega \qquad (V_m \omega)$$

The maximum rate at which the output changes, occures as the curves cross the zero axis.

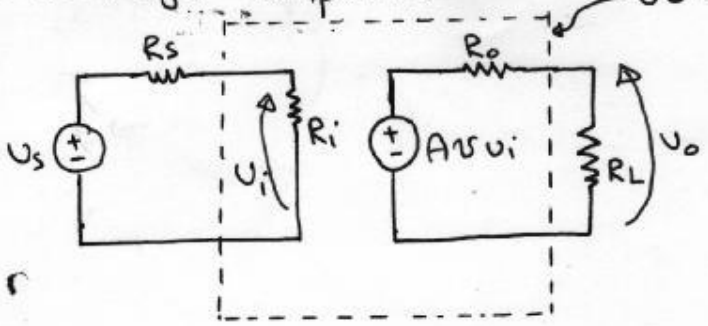
If $(\omega V_m) > SR$, then the o/p is distorted.

$$f_{max} = \frac{SR}{V_m 2\pi}$$ (f_{max} is the maximum frequency without distortion of the output).

as V_m changes, f_{max} changes.

Classification of amplifiers:- (Feed back)

1- Voltage amplifier



$R_i >> R_s$

$R_o << R_L$

Ideally, $R_i = \infty$

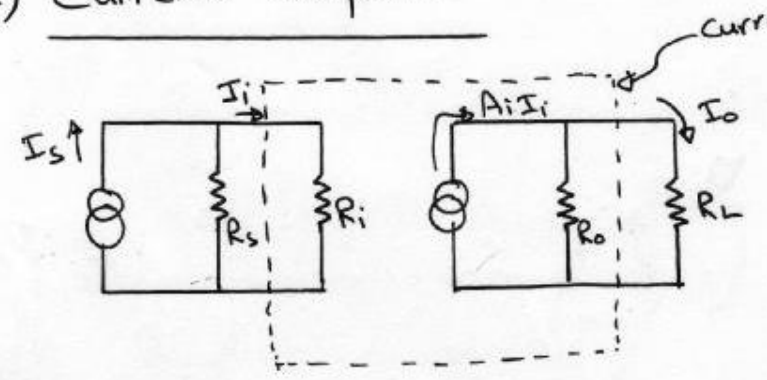
$R_o = 0$

$\therefore V_o = A_v v_i = A_v V_s$

$$\frac{V_o}{V_s} = A_v$$

the output voltage is proportional to the input voltage independently of R_L and R_s.

2) Current amplifier



$R_i << R_s$

$R_o >> R_L$

Ideally, $R_i = 0$

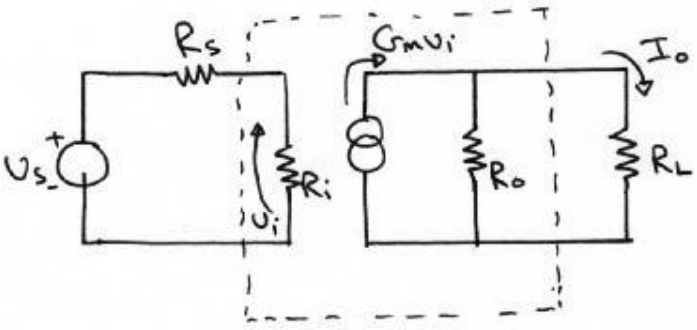
$R_o = \infty$

$I_o = A_i I_i = A_i I_s$

$\frac{I_o}{I_s} = A_i$

The output current is proportional to the input current and the proportionality constant is independent of R_L and R_s.

3) Transconductance amplifier:-



G_m is the transconductance of the amplifier

$R_o \gg R_L$

$R_i \gg R_s$

Ideally $R_i = \infty$

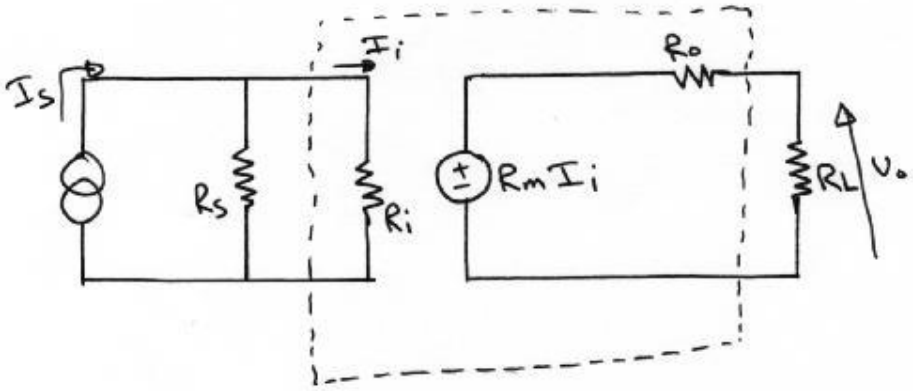
$R_o = \infty$

$I_o = G_m V_i = G_m V_s$

$\frac{I_o}{I_s} = G_m$

The output current is proportional to the input voltage independently of R_s and R_L.

(4) Transresistance amplifier:-



$R_i \ll R_s$

$R_o \ll R_L$

Ideally:-

$R_i = 0$

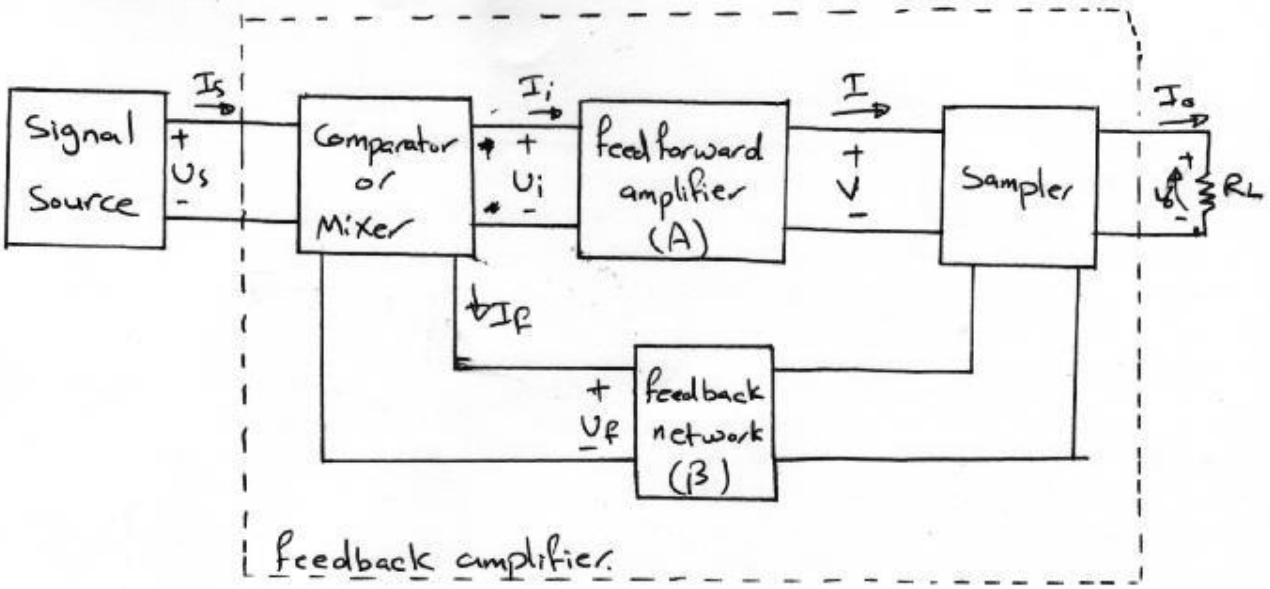
$R_o = 0$

$V_o = R_m I_i = R_m I_s$

$\frac{V_o}{I_s} = R_m$

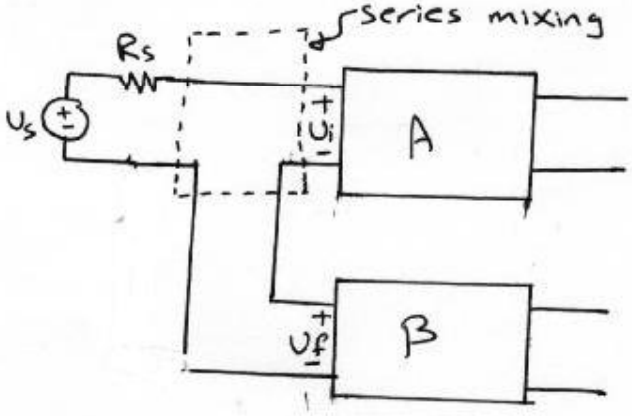
The output voltage is proportional to the input current independently of R_s and R_L.

The feed back Concept :-



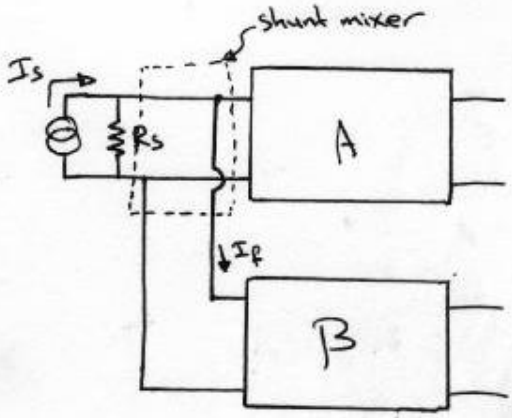
Mixers or Comparators

(1)



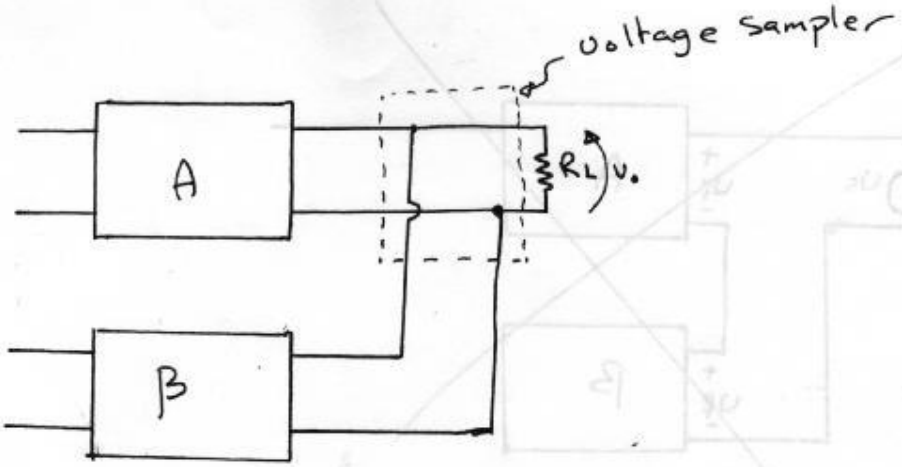
Series mixing

(2)

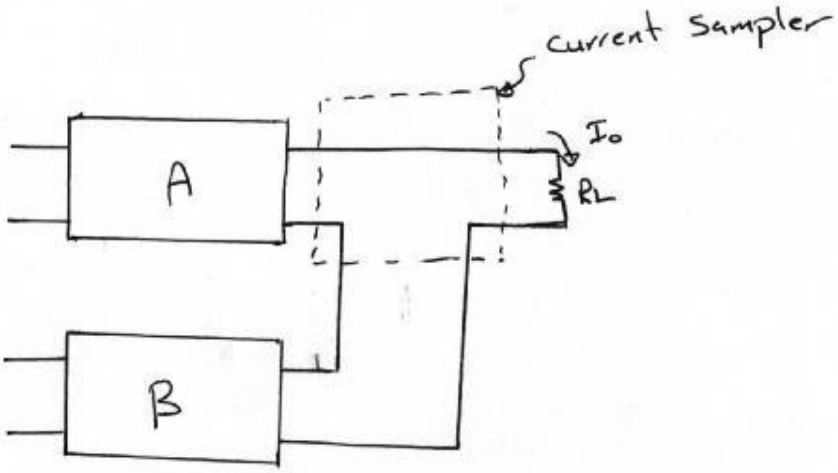


Shunt mixing

Samplers :-

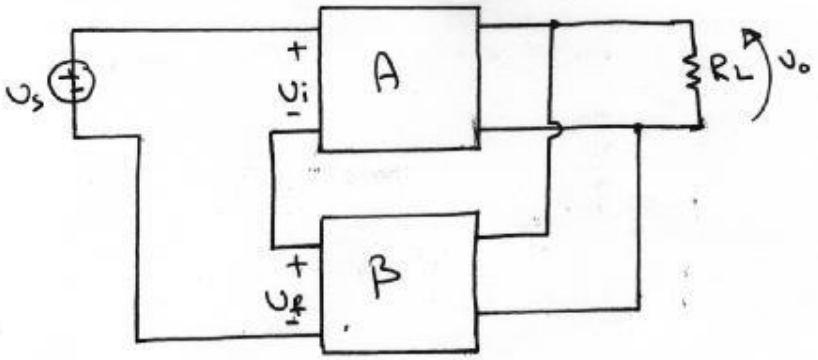


Voltage sampling or node sampling

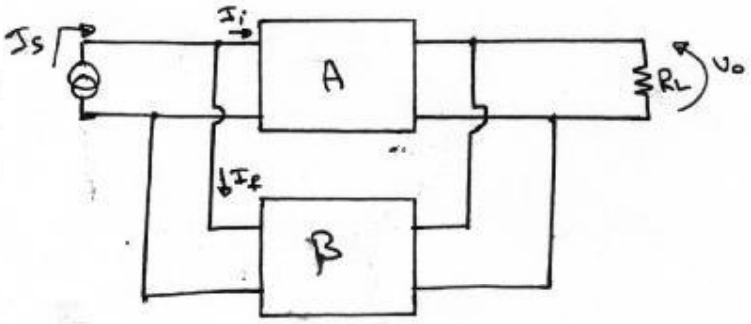


Current sampling or loop sampling

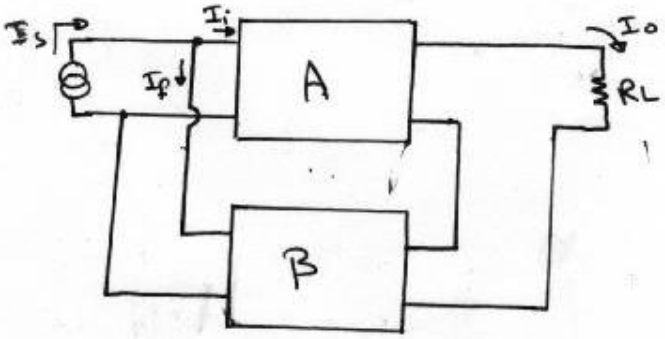
Feedback amplifier topologies:-



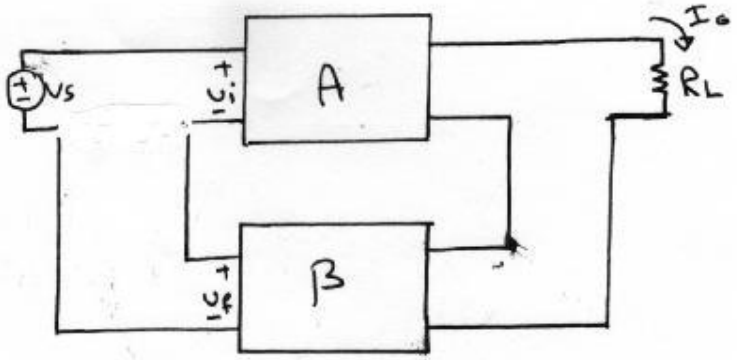
Voltage - series feedback circuit.



Voltage-shunt f.b.



Current - shunt f.b.



Current-series f.b.

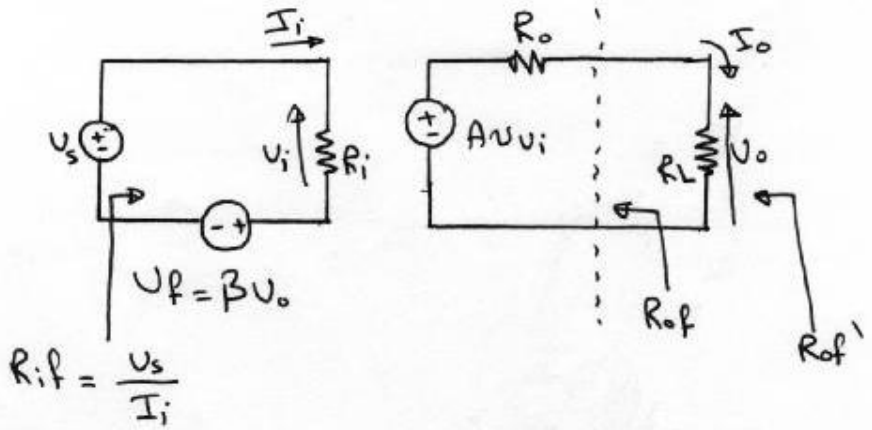
Input Resistance:-

$R_{if} > R_i$ for series mixing whether sampling is voltage or current.

$R_{if} < R_i$ for shunt mixing whether sampling is voltage or current.

Input resistance:-

1- Voltage-series feedback



Fig(a): Voltage-series f.b. cct. used to find R_{if}, R_{of}, and R_{of}'.

$$V_s = V_i + V_f$$
$$= V_i + \beta V_o$$

$$V_o = \frac{A_V V_i R_L}{R_o + R_L} = A_V V_i$$

where

$$A_V = \frac{A_V R_L}{R_o + R_L} = \frac{V_o}{V_i}$$

$$V_s = V_i + \beta A_V V_i$$

$$V_s = V_i (1 + \beta A_V)$$
$$= I_i R_i (1 + \beta A_V)$$

$$R_{if} = \frac{V_s}{I_i} = R_i (1 + \beta A_V)$$

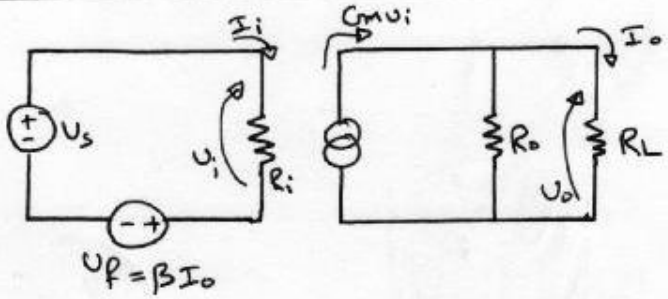
$$R_{if} = R_i D$$
$$\therefore \quad R_{if} > R_i$$

A_V is the open ckt. voltage gain without f.b..

A_V is the voltage gain without feedback but taking R_L into account.

$$A_V = \lim_{R_L \to \infty} A_V$$

2. Current - Series f.b. :-



Fig(b) current - series f.b. ckt.

$$V_s = V_i + V_f$$
$$= V_i + \beta I_o$$

$$I_o = \frac{G_m V_i R_o}{R_o + R_L} = G_M V_i$$

where $$G_M = \frac{G_m R_o}{R_o + R_L} = \frac{I_o}{V_i}$$

$$V_s = V_i + \beta G_M V_i$$
$$= V_i (1 + \beta G_M) = I_i R_i (1 + \beta G_M)$$

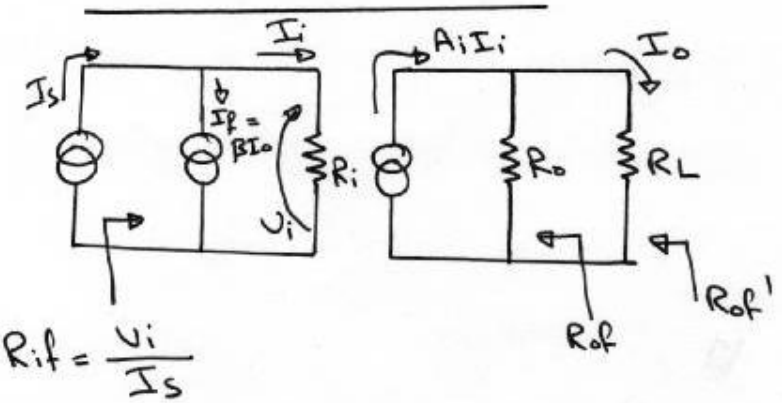
$$R_{if} = \frac{V_s}{I_i} = R_i (1 + \beta G_M) = R_i D.$$

$$R_{if} = R_i D$$

$$R_{if} > R_i$$

$$G_m = \lim_{R_L \to 0} G_M .$$

3- Current-shunt f.b.:-



$$R_{if} = \frac{V_i}{I_s}$$

Figure (c):- Current-shunt f.b. cct. used to calculate R_{if}, R_{of} and R_{of}'.

$$I_s = I_i + I_f$$
$$= I_i + \beta I_o$$

$$I_o = \frac{A_i I_i R_o}{R_o + R_L} = A_I I_i$$

where $A_I = \frac{A_i R_o}{R_o + R_L}$

$$I_s = I_i + \beta A_I I_i = I_i (1 + \beta A_I).$$

$$I_s = \frac{V_i}{R_i}(1 + \beta A_I)$$

$$R_{if} = \frac{V_i}{I_s} = \frac{R_i}{1 + \beta A_I} = \frac{R_i}{D}$$

$\therefore R_{if} < R_i$

$$A_i = \lim_{R_L \to \infty} A_I .$$

4 - Voltage - shunt f.b. :-

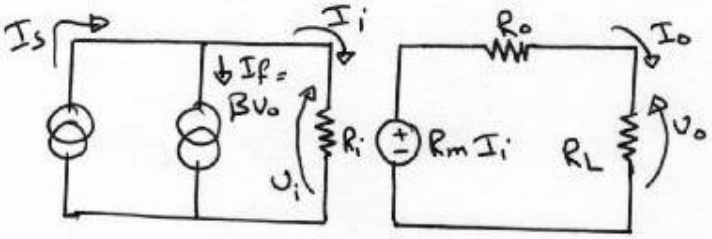


fig. (d) Voltage - shunt f.b. circuit.

$$I_s = I_i + I_f$$
$$= I_i + \beta V_o$$

$$V_o = \frac{R_m I_i R_L}{R_o + R_L} = R_M I_i$$

where $R_M = \frac{R_m R_L}{R_o + R_L}$

$$I_s = I_i + \beta R_M I_i$$

$$I_s = \frac{V_i}{R_i}(1+\beta R_M)$$

$$R_{if} = \frac{R_i}{1+\beta R_M} = \frac{R_i}{D}$$

$\therefore R_{if} < R_i$

$$R_M = \lim_{R_L \to \infty} R_M .$$

Output resistance:-

$R_{of} < R_o$ for voltage sampling

$R_{of} > R_o$ for current sampling

How to find the output resistance?

(a) Open the o/p cct. (disconnect R_L) and impress a voltage source V instead which causes a current I to flow.

(b) Set $V_s = 0$ for series mixing and $I_s = 0$ for shunt mixing.

(c) Find $R_{of} = \frac{V}{I}$

(d) Find $R_{of}' = R_{of} \parallel R_L$

1- Voltage series:-

Applying the above four steps to figure (a), we find :-

$$R_{of} = \frac{R_o}{(1+\beta A_v)} \neq D$$

$$R_{of}' = \frac{R_o'}{1+\beta A_v}$$

$$R_{of}' = \frac{R_o'}{D}$$

where $R_o' = R_o \| R_L$

$\therefore R_{of} < R_o$

$R_{of}' < R_o'$

2- Voltage shunt f.b.:-

$$R_{of} = \frac{R_o}{1+\beta R_m}$$

$$R_{of}' = \frac{R_o'}{1+\beta R_M} = \frac{R_o'}{D}$$

$R_{of} < R_o$

$R_{of}' < R_o'$.

3- Current - shunt f.b.:-

Refer to fig(b) we obtain:-

$$R_{of} = R_o(1+\beta A_i)$$

$$R_{of}' = R_o' \frac{(1+\beta A_i)}{(1+\beta A_I)}$$

$R_{of} > R_o$

$R_{of}' > R_o'$

4- Current- Series f.b. :-

$$R_{of} = R_o(1+\beta G_m)$$

$$R_{of}' = \frac{R_o'(1+\beta G_m)}{(1+\beta G_M)}$$

$\therefore R_{of} > R_o$

$R_{of}' > R_o'$.

Specifying the topology:-

To know the topology we must first locate the i/p loop which is the mesh containing the applied signal V_s and either
(a) the base-to-emitter region of the first bipolar transistor, or
(b) the gate-to-source region of the first FET in the amplifier or
(c) the section between the two inputs of a diff. amp.

Also the i/p node which is (a) the base of the first BJT or (b) the gate of the first FET or (c) the inverting terminal of a differential amp.

To know the mixing type as following:-

The mixing is series if in the i/p cct. there exist a circuit component γ in series with V_s and if γ is connected to the output (the portion of the system containing the load). If this condition is true, the voltage across γ is the feedback signal $X_f = V_f$.

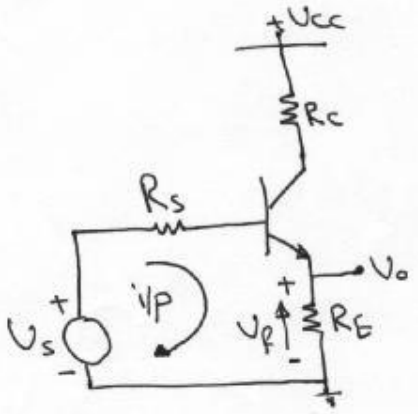
If the above is not satisfied, we must test for shunt mixing. The mixing is shunt if there is a connection between the i/p node and the o/p circuit. The current in this connection is the feedback signal $X_f = I_f$.

To know the sampling type then:-

These are the tests for the type of sampling:-

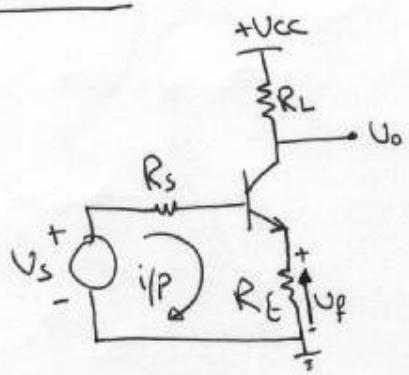
1. Set $V_o = 0$ (that is, set $R_L = 0$). If X_f becomes zero, the original system has voltage sampling.
2. Set $I_o = 0$ (that is, set $R_L = \infty$). If X_f becomes zero, current sampling was present in the original system.

Example (1)



Voltage-series f.b. amp.

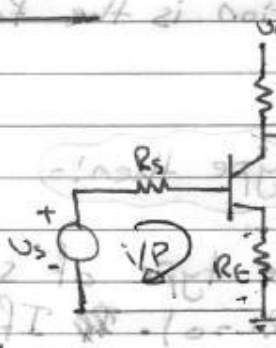
Example (2)



Current-Series f.b. amp.

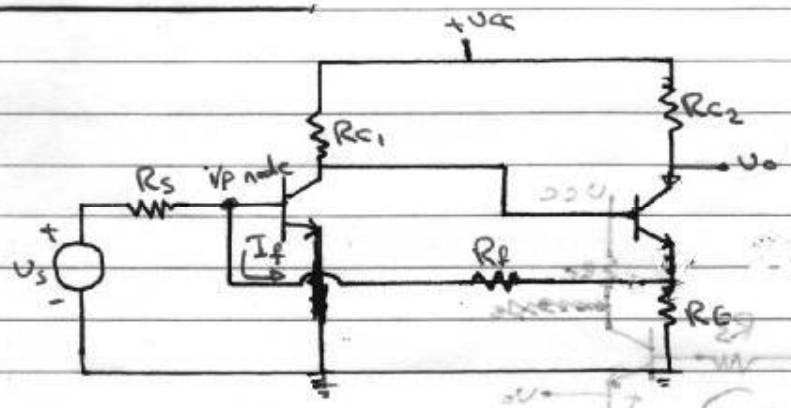
Subject : Date:

Example (2)



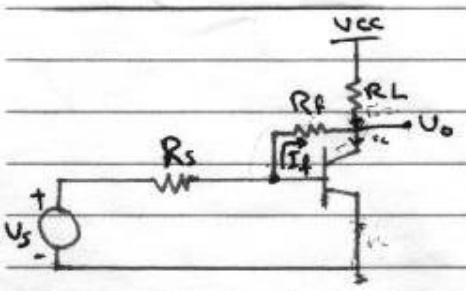
Current-series f.b. amp

Example (3)



Current-shunt f.b amp

Example (4)



Voltage-shunt f.b amp

Subject : Date:

Method of analysis of a feedback amplifier:-

The amplifier without feedback :-

To find the input circuit:-

1. Set $V_o = 0$ for voltage sampling. In other words, short-circuit the output node;
2. Set $I_o = 0$ for current sampling. In other words, open-circuit the output loop.

To find the output circuit:-

1. Set $V_i = 0$ for shunt mixing. In other words, short circuit the input node (so that none of the feedback current enters the amplifier input).
2. Set $I_i = 0$ for series mixing. In other words, open-circuit the input loop (so that none of the feedback voltage reaches the amplifier input).

Outline of Analysis

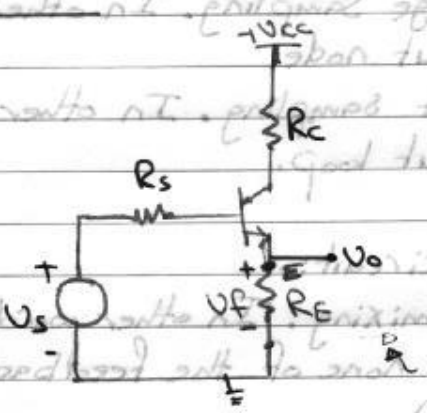
To find A_f, R_{if}, and R_{of} the following steps are carried out:-

1. Identify the topology.
2. Draw the basic amplifier circuit without feedback, following the above rules.
3. Use a Thevenin's source if X_f is a voltage and a Norton's source if X_f is a current.
4. Replace each active device by its proper model.
5. Calculate $\beta = \frac{X_f}{X_o}$

Subject : Date:

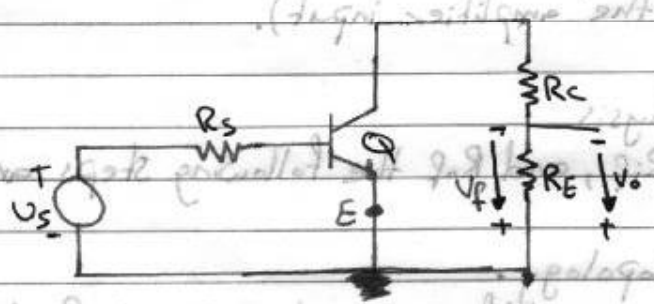
6- Calculate A.
7- from A and β, find D, A_f, R_{if}, R_{of}, and R_{of}'.

Example (1)

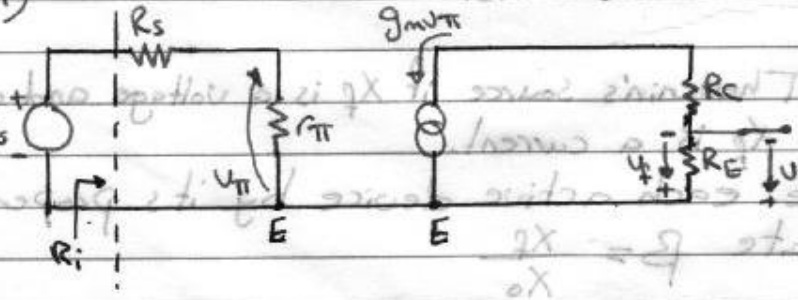


1) Voltage-series f.b.

2)



3 and 4)



Subject : Date:

5) $\beta = \frac{X_f}{X_o} = \frac{V_f}{V_o} = 1$

6) A

in this example A is A_V

$$A_V = \frac{V_o}{V_s} = \frac{g_m V_\pi R_E}{V_\pi} \cdot \frac{r_\pi}{r_\pi + R_s} = \frac{\beta_o R_E}{r_\pi + R_s}$$

7) find D, A_f, R_{if}, R_{of}, and R_{of}'.

$$D = 1 + \beta A_V$$

$$= 1 + \frac{\beta_o R_E}{r_\pi + R_s} = \frac{r_\pi + R_s + \beta_o R_E}{r_\pi + R_s}$$

$$A_{Vf} = \frac{A_V}{D} = \frac{\beta_o R_E}{r_\pi + R_s + \beta_o R_E}$$

for $(\beta_o R_E) \gg r_\pi + R_s$

$A_{Vf} \approx 1$

This type of feedback desensitizes the voltage gain against β_o variations.

$R_i = r_\pi + R_s$

$R_{if} = R_i D$

$R_{if} = r_\pi + R_s + \beta_o R_E$.

Subject : Date:

$R_o = \infty$

$R_{of} = \dfrac{R_o}{1+\beta A_V}$

$A_V = \lim_{R_L \to \infty} A_V$

$R_L = R_E$

$A_V = \infty$

$\therefore R_{of} = \dfrac{\infty}{\infty}$

$R_{of}' = \dfrac{R_o'}{D}$

$R_o' = R_o \,//\, R_L$

$= \infty \,//\, R_E$

$= R_E$

$\therefore R_f' = \dfrac{(r_\pi + R_s)\, R_E}{r_\pi + R_s + \beta_o R_E}$

$R_{of}' = R_{of} \,//\, R_E$

Therefore $R_{of} = \lim_{R_E \to \infty} R_{of}'$

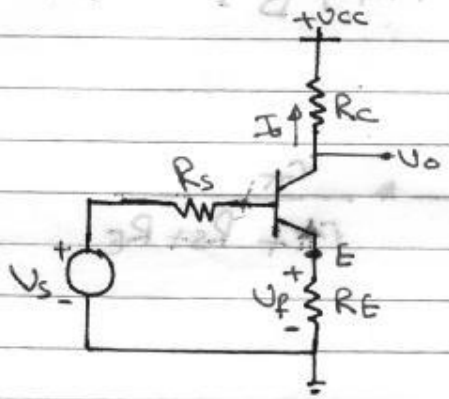
$\therefore R_{of} = \dfrac{r_\pi + R_s}{\beta_o}$

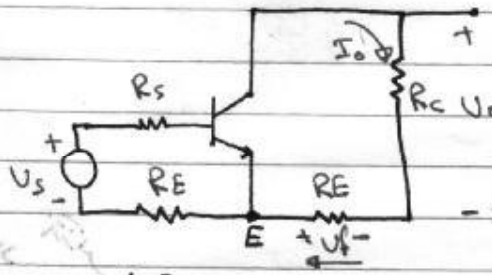
In the feedback method we assume zero forward transmission through the β-network. In the CC amplifier, such is not the case since a forward current (the base current) also flows through R_E. Therefore the expressions for R_{of} and R_{if} have $(\beta_o + 1)$ replaced by β_o.

Subject : Date:

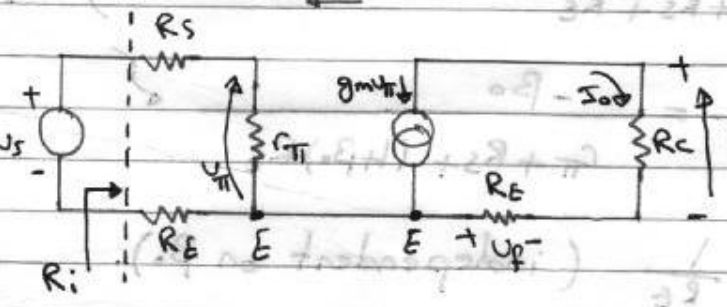
2) Current - series feedback:-

The CE amplifier (Example 2):-





amplifier without f.b



$$* \beta = \frac{X_f}{X_o} = \frac{V_f}{I_o} = \frac{-R_E I_o}{I_o}$$

$$\beta = -R_E$$

Subject : Date:

This is a transconductance amplifier So:-

$A = G_M$.

* $A_{vf} \neq \frac{A_v}{D}$ فإن A_{vf} طلب إذا

∴ دائما

$$* G_{Mf} = \frac{G_M}{D}$$

$$* G_M = \frac{I_o}{V_s} = \frac{-g_m v_\pi}{v_\pi} * \frac{r_\pi}{r_\pi + R_s + R_E}$$

$$G_M = \frac{-\beta_o}{r_\pi + R_s + R_E}$$

$$* D = 1 + \beta G_M$$

$$= 1 + \frac{\beta_o R_E}{r_\pi + R_s + R_E}$$

$$D = \frac{r_\pi + R_s + (1+\beta_o) R_E}{r_\pi + R_s + R_E}$$

$$* G_{Mf} = \frac{G_M}{D} = \frac{-\beta_o}{r_\pi + R_s + (1+\beta_o) R_E}$$

تتأثر

$$\therefore G_{Mf} \approx -\frac{1}{R_E} \quad \text{(independent on } \beta_o\text{)}.$$

This type of feedback desensitizes the transconductance against β_o variations.

Subject : Date:

$$* A_{Vf} = \frac{V_o}{V_s} = \frac{I_o R_L}{V_s} = G_{Mf} R_L$$

$R_L = R_C$

$$A_{Vf} = \frac{-\beta_o R_C}{r_\pi + R_S + (1+\beta_o) R_E} \approx \frac{-R_C}{R_E}$$

$$* R_i = R_S + r_\pi + R_E$$

$$R_{if} = R_i D$$

$$= r_\pi + R_S + (1+\beta_o) R_E .$$

$$* R_o = \infty \quad , G_m = \lim_{R_L \to \infty} G_M * = G_M$$

$$R_{of} = R_o (1 + \beta G_m)$$

$$= \infty .$$

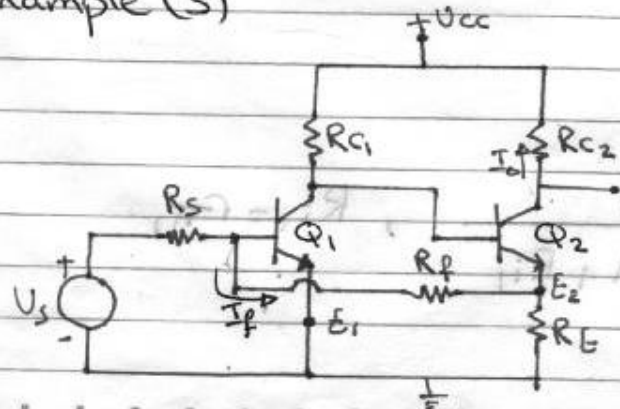
$$* R_{of}' = R_{of} // R_L$$

$$= \infty // R_C$$

$$= R_C .$$

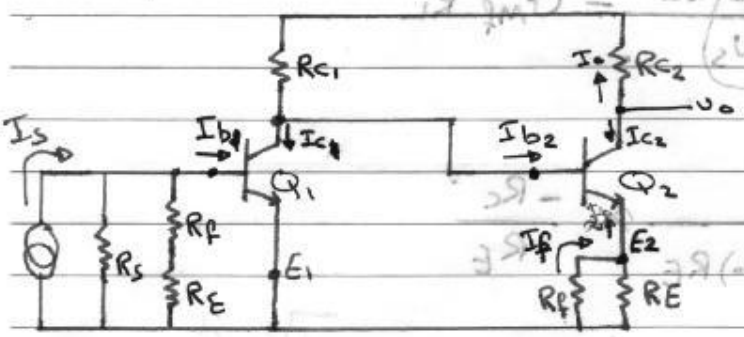
③ Current-shunt feedback :-

Example (3)



Subject : Date:

amplifier without f.b.



$$* \beta = \frac{I_f}{I_o} = \frac{R_E}{R_f + R_E}$$

in this example A is A_I

$$* A_I = \frac{I_o}{I_s} = \frac{I_o}{I_{b_2}} \cdot \frac{I_{b_2}}{I_{c_1}} \cdot \frac{I_{c_1}}{I_{b_1}} \cdot \frac{I_{b_1}}{I_s}$$

$$\frac{I_o}{I_{b_2}} = -h_{fe}$$

$$\frac{I_{b_2}}{I_{c_1}} = -\frac{R_{c_1}}{R_{c_1} + R_{i_2}}$$

$$R_{i_2} = (R_E \| R_f)(1+\beta_o) + r_{\pi_2}$$

$$\frac{I_{c_1}}{I_{b_1}} = h_{fe}$$

$$\frac{I_{b_1}}{I_s} = \frac{R_s \| (R_f + R_E)}{R_s \| (R_f + R_E) + R_{i_1}}, \quad R_{i_1} = r_{\pi_1}$$

$A_I = \checkmark$

Subject : Date :

$*D = 1 + \beta A_I$

$*A_{If} = \frac{A_I}{D} = \frac{I_o}{I_s}$

$A_{vf} = \frac{V_o}{V_s} = \frac{I_o R_L}{I_s * R_s} = A_{If} * \frac{R_{c2}}{R_s}$

$*R_{if} = \frac{R_i}{D}$

$R_i = R_s // (R_f + R_E) // r_{\pi_1}$

$R_{if} = \frac{R_i \checkmark}{D -} = \checkmark$

$*R_{of} = R_o(1 + \beta A_i)$

$R_o = \infty$

$A_i = \lim_{R_L \to \infty} A_I = A_I$

$R_{of} = \infty$

$*R_{of}' = R_o' \frac{1 + \beta A_i}{1 + \beta A_I}$

$R_o' = R_o // R_L \quad , R_L = R_{c2}.$

$R_o' = \infty // R_{c2}$

$R_o' = R_{c2}$

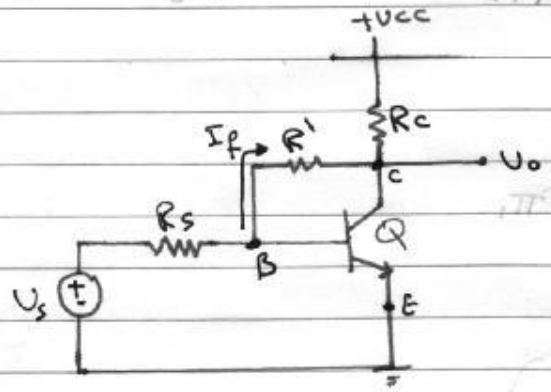
$A_i = \lim_{\substack{R_L \to \infty \\ R_{c2} \to \infty}} A_I = A_I.$

Subject : Date:

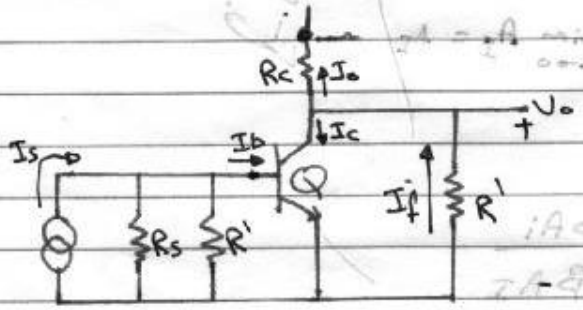
$R_{of}' = R_{C_2}$.

4) Voltage_Shunt f.b :-

Example (4)



amplifier without f.b



$$* \beta = \frac{I_f}{V_o} = \frac{-1}{R'}$$

in this example A is R_M.

$$* R_M = \frac{V_o}{I_s} = \frac{V_o}{I_c} * \frac{I_c}{I_b} * \frac{I_b}{I_s}$$

$$= -(R' // R_c) * h_{fe} * \frac{R_s // R'}{R_s // R' + R_{in}}, \quad R_{in} = r_\pi$$

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$$\therefore R_M = -(R' // R_c) * h_{fe} * \frac{R_s // R'}{R_s + R' + r_\pi}$$

* $D = 1 + \beta R_M = \checkmark$

* $R_{Mf} = \frac{R_M}{D} = \checkmark$

* $A_{Vf} = \frac{V_o}{V_s} = \frac{V_o}{I_s * R_s} = \frac{R_{Mf}}{R_s}$

* $R_{if} = \frac{R_i}{D}$

$R_i = R_s // R' // r_\pi$

$R_{if} = \checkmark$

* $R_o = R'$

$R_{of} = \frac{R_o}{1 + \beta R_m}$, $R_m = \lim_{\substack{R_L \to \infty \\ R_s \to \infty}} R_M$

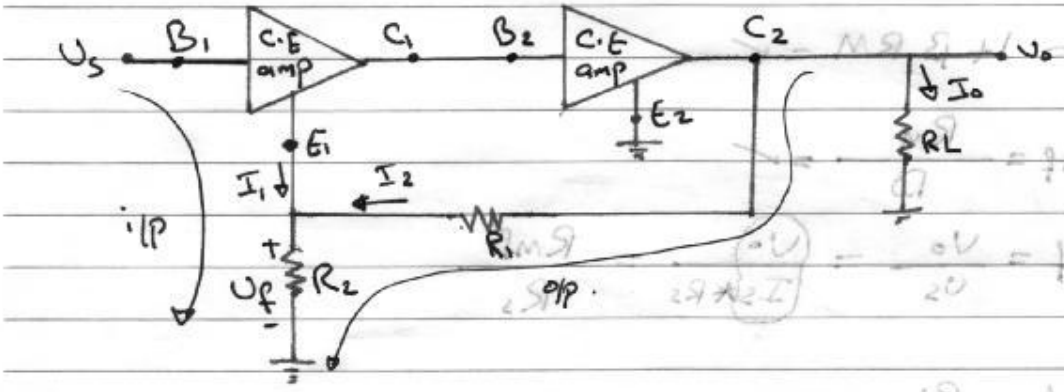
$R_{of} = \checkmark$

* $R_o' = R_o // R_L$
$= R' // R_c$

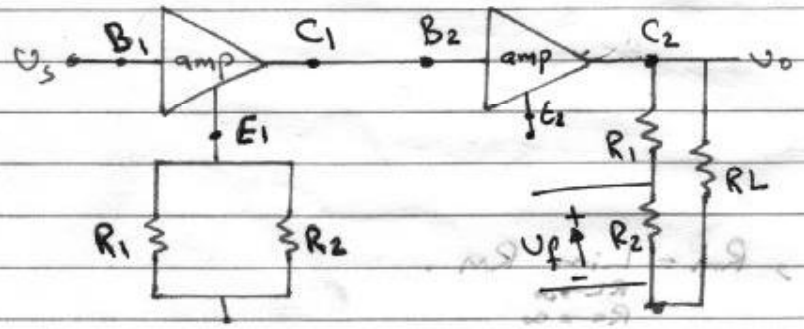
$R_{of}' = \frac{R_o'}{D} = \checkmark$.

Subject : Date:

Example:-
The voltage-series feedback pair (second Collector to first emitter feedback).



amp. without feedback



$$\beta = \frac{R_2}{R_1+R_2} = \frac{v_f}{v_o}$$

$$A_v = A_{v_1} A_{v_2}$$
$$D = 1 + \beta A_v$$
$$A_{vf} = \frac{A_v}{D}.$$

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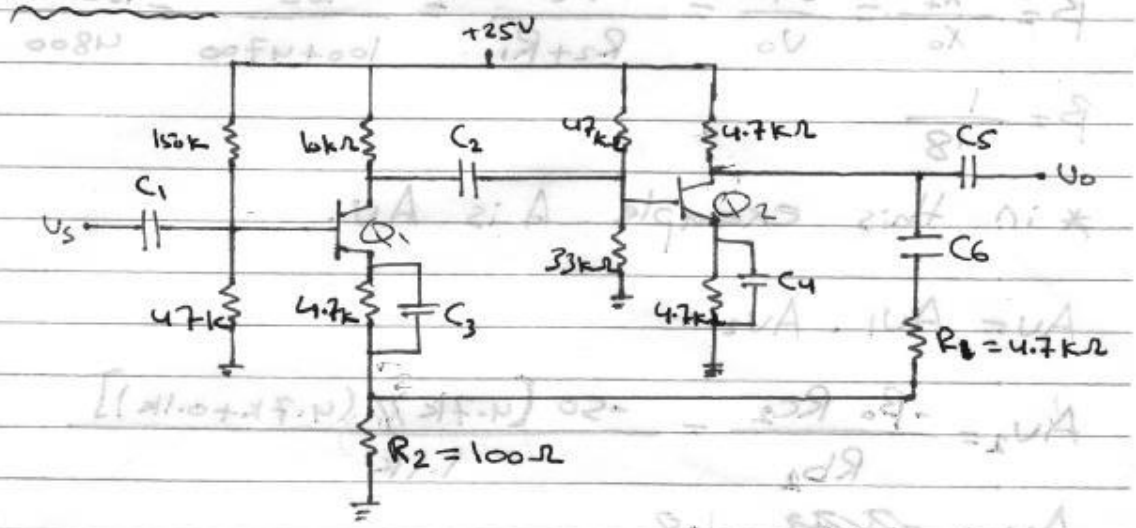
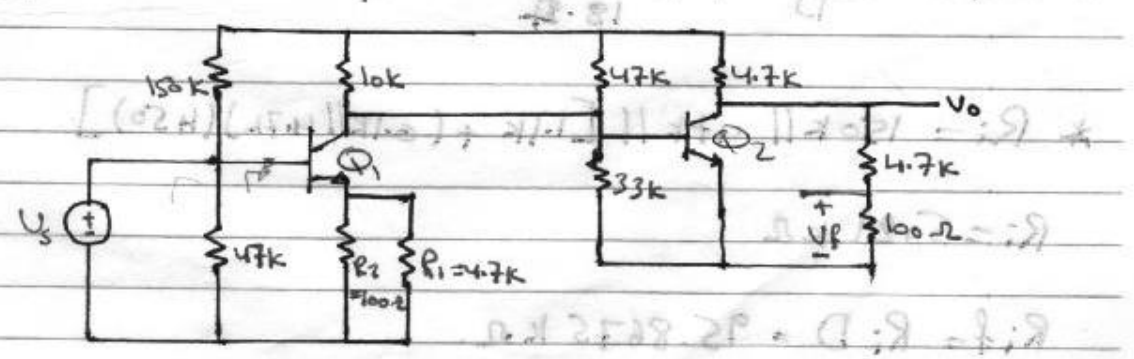
Example:



This circuit shows a two-stage amplifier which makes use of voltage-series feedback by connecting the second collector to the first emitter through the voltage divider R_1R_2. Capacitors C_1, C_2, C_5 and C_6 are d.c blocking capacitors, and capacitors C_3 and C_4 are bypass capacitors.

Calculate A_{vf}, R_{of} and R_{if} for the amplifier. Assume $R_S = 0$, $\beta_o = 50$, $r_\pi = 1.1k\Omega$ and identical transistors.

Sol:- The amplifier without feedback.



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$$\beta = \frac{x_f}{x_o} = \frac{v_f}{v_o} = \frac{R_2}{R_2 + R_1} = \frac{100}{100 + 4700} = \frac{100}{4800}$$

$$\beta = \frac{1}{48}$$

* in this example A is A_V.

$$A_V = A_{V1} \cdot A_{V2}$$

$$A_{V2} = \frac{-\beta_o R_{C2}}{R_{b2}} = \frac{-50\,[4.7k \,//\, (4.7k + 0.1k)]}{1.1k}$$

$$A_{V2} = -108$$

$$A_{V1} = \frac{-\beta_o R_{C1}}{R_{b1}} = \frac{-50\,(10k \,//\, 47k \,//\, 33k \,//\, 1.1k)}{1.1k + (0.1k \,//\, 4.7k)(50)}$$

$$A_{V1} = -7.73$$

$$A_V = A_{V1} * A_{V2} = -7.73 * -108 = 835$$

* $D = 1 + \beta A_V$

$$D = 1 + \frac{835}{48} = 18.4$$

* $A_{Vf} = \frac{A_V}{D} = \frac{835}{18.4} = 45.4$

* $R_i = 150k \,//\, 47k \,//\, [1.1k + (0.1k \,//\, 4.7k)(50)]$

$$R_i = 5.21\,k\Omega$$

$$R_{if} = R_i D = 95.8675\,k\Omega$$

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* $R_{of}' = \frac{R_o'}{D}$

$R_o' = 4.7k \,//\, (4.7k + 0.1k)$

$= 2.37k\Omega$.

$R_{of}' = \frac{2.37k}{18.4} = 129\Omega$.

Oscillators :-

Linear Oscillators :-

An oscillator generates a periodic output without requiring any input.

Oscillators

- Linear (sinusoidal)
- non linear (square, triangular)

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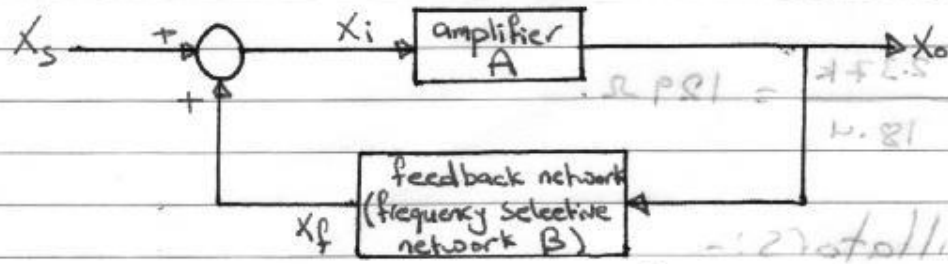
Basic principles of sinusoidal oscillators:-

① The oscillator feedback loop.



The basic structure of a sinusoidal oscillator.

The frequency selective network determines the frequency of oscillation.

This is a +ve feedback structure its equations are:-

$$X_o = A X_i \quad \text{---} ①$$

$$X_f = \beta X_o \quad \text{---} ②$$

$$X_i = X_s + X_f \quad \text{---} ③$$

Solving the above equations for $A_f = \frac{X_o}{X_s}$ we get:-

$$A_f = \frac{A}{1 \ominus \beta A}$$

↓ The $\ominus$ sign is for +ve feedback.

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$$A_f(s) = \frac{A(s)}{1 - \beta(s) A(s)}$$

in general A does not depend on frequency.

$\beta(s)$ depends on frequency since it contains reactive elements.

the loop gain is βA.

② The Oscillation Criterian :-

If at a specific frequency the loop gain $\beta A = 1$ then :-

$$1 - \beta A = 0$$

and $A_f = \infty$

This means that we have a finite output for zero input which is by definition an oscillator.

Therefore the circuit oscillates at a frequency ω_o if :-

$$\boxed{A(j\omega_o)\,\beta(j\omega_o) = 1}$$

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The Barkhausen criterian for oscillation is:-

1- $|A(j\omega_o)\,\beta(j\omega_o)| = 1$

2- $\angle A(j\omega_o)\,\beta(j\omega_o) = 0°$

By this we have:-

$A\beta = 1$

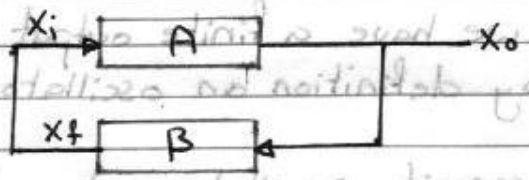
$X_o = A X_i$

$X_f = \beta X_o$

$\therefore X_f = A\beta X_i$, $A\beta = 1$

$\therefore \boxed{X_f = X_i}$ (no input).

$\therefore$



let

$|A\beta|$ 5% greater than unity to start and maintain Oscillation.

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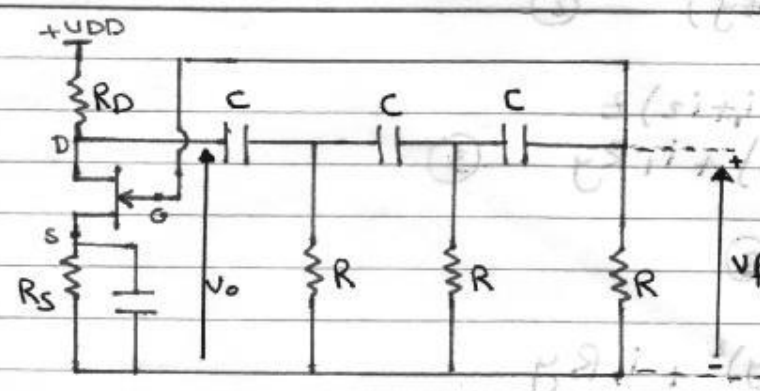
The FET phase-shift oscillator:-



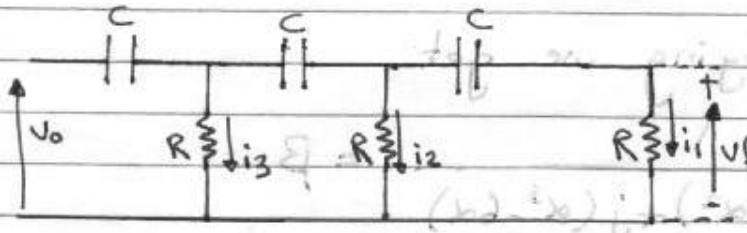
To find the frequency of oscillation:-

$A(j\omega)\beta(j\omega) > 1$

① find $\beta(j\omega) = ?$ $\beta = \frac{v_f}{v_o}$

② Set the imaginary part = 0 and derive f_{osc}.

so for this circuit we have:-



let $Z = \frac{1}{j\omega C}$ and $y = \frac{Z}{R}$ and $\alpha = \frac{1}{\omega CR}$

$V_f = i_1 R$ ——①

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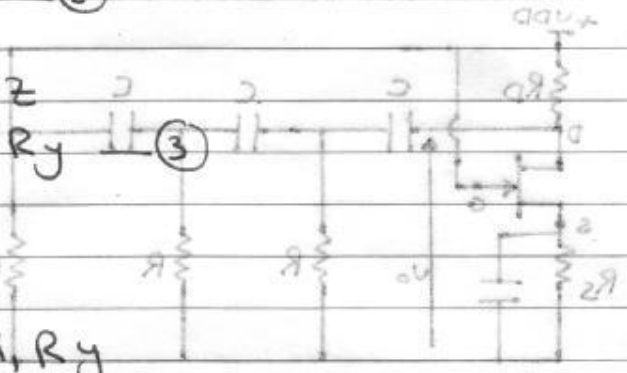
$i_2 R = i_1 (R + z)$

$i_2 R = i_1 R (1+y)$ ——②



$i_3 R = i_2 R + (i_1 + i_2) z$

$i_3 R = i_2 R (1+y) + i_1 R y$ ——③

sub ② in ③

$i_3 R = i_1 R (1+y)^2 + i_1 R y$

$i_3 R = i_1 R ((1+y)^2 + y)$ ——④

$v_o = i_3 R + (i_1 + i_2 + i_3) z$

$v_o = i_3 R (1+y) + i_1 R y + i_2 R y$ ——⑤

sub ④ and ② in ⑤ we get

$v_o = i_1 R ((1+y)^2 + y)(1+y) + i_1 R y + i_1 R (1+y) y$

after simplifying we get

$$\frac{v_f}{v_o} = \frac{}{(1-5\alpha^2) + j(\alpha^3 - 6\alpha)}$$

to find ω_{osc} set the imaginary part = 0

$\alpha^3 - 6\alpha = 0 \Rightarrow \alpha = \sqrt{6}$, $\alpha = \frac{1}{\omega CR}$

$$\frac{1}{\omega_{osc} CR} = \sqrt{6} \Rightarrow \omega_{osc} = \frac{1}{\sqrt{6}\, CR}$$

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$$f_{osc} = \frac{1}{2\pi\sqrt{6}\,CR}$$

$|AB| > 1$

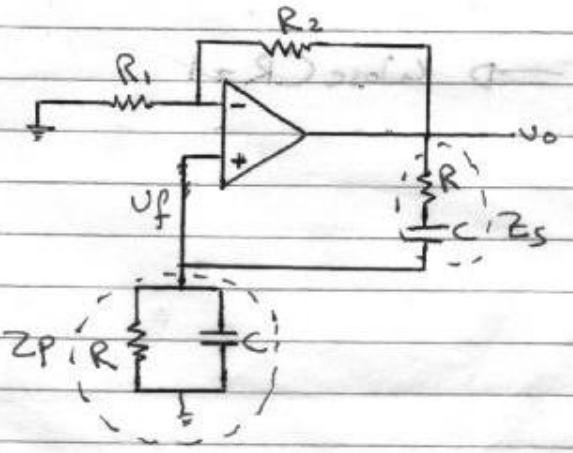
at f_{osc}

$$\beta = \frac{1}{1-5\alpha^2} = \frac{-1}{29}$$ -ve and real

$$|A| \geq \frac{1}{|B|} \quad \therefore |A| > -29$$

$$A = \frac{-\mu R_D}{r_d + R_D} \quad \therefore \frac{-\mu R_D}{r_d + R_D} > -29$$

The Wien bridge Oscillator:-



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$$A(s)\,\beta(s) = \left(1+\frac{R_2}{R_1}\right)\left(\frac{Z_p}{Z_p+Z_s}\right)$$

$$= \left(1+\frac{R_2}{R_1}\right)\left[\frac{\frac{R}{1+SCR}}{\frac{R}{1+SCR}+R+\frac{1}{SC}}\right]$$

$$= \left(1+\frac{R_2}{R_1}\right)\left(\frac{1}{3+SCR+\frac{1}{SCR}}\right)$$

$$A(j\omega)\,\beta(j\omega) = \left(1+\frac{R_2}{R_1}\right)\left[\frac{1}{3+j\left(\omega CR-\frac{1}{\omega CR}\right)}\right]$$

At ω_{osc}, imaginary part = 0

$$\omega_{osc}CR - \frac{1}{\omega_{osc}CR} = 0$$

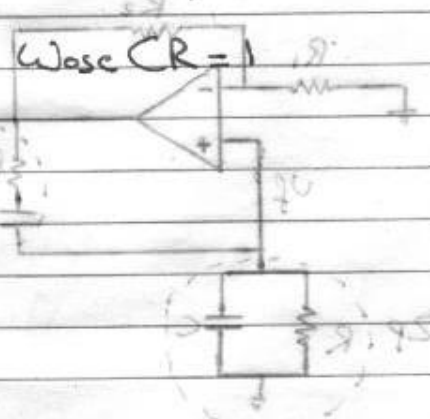
$$\left[\omega_{osc}CR\right] = \frac{1}{\omega_{osc}CR} \Rightarrow \omega_{osc}CR = 1$$

$$\omega_{osc} = \frac{1}{CR}$$

$$f_{osc} = \frac{1}{2\pi CR}$$

At ω_{osc}

$$A\beta = \left(1+\frac{R_2}{R_1}\right)\left(\frac{1}{3}\right)$$



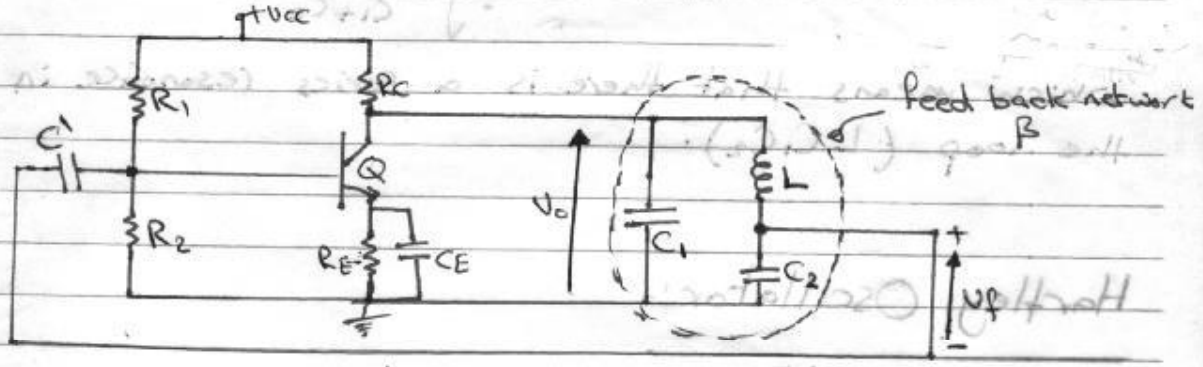
Subject :

$|AB| > 1$

$\left(1 + \frac{R_2}{R_1}\right)\left(\frac{1}{3}\right) > 1 \Rightarrow \frac{R_2}{R_1} > 2.$

LC oscillators:-

1- The transistor colpitts oscillator:-



$$\frac{V_f}{V_o} = \beta = \frac{\frac{1}{SC_2}}{\frac{1}{SC_2} + SL} = \frac{1}{1 + S^2 LC_2}$$

$C_1, C_2 \ll C'_{C_E}$

$$A = \frac{V_o}{V_\pi} = \frac{-g_m V_\pi \left(R \,//\, \frac{1}{SC_1} \,//\, \left(\frac{1}{SC_2} + SL\right)\right)}{V_\pi}$$

i.e. V_{BE}.

After simplification:-

$$A\beta = -g_m \frac{R(S^2 LC_2 + 1)}{SRC_2 + (SRC_1 + 1)(S^2 LC_2 + 1)} * \frac{1}{(1 + S^2 LC_2)}$$

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$$A(j\omega)\beta(j\omega) = -g_m R\left(\frac{1}{j\omega RC_2 - j\omega^3 RLC_1C_2 + j\omega RC_1 - \omega^2 LC_2 + 1}\right)$$

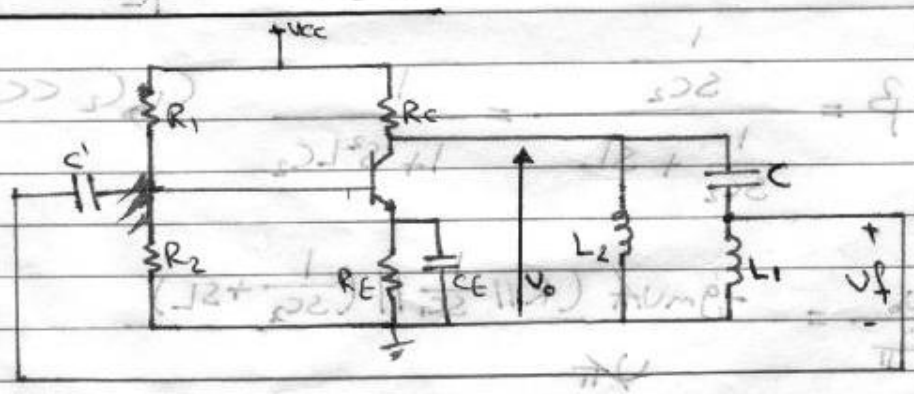
at ω_{osc}, imaginary part = 0

$$\omega_{osc} RC_2 + \omega_{osc} RC_1 - \omega_{osc}^3 RLC_1C_2 = 0$$

$$C_2 + C_1 = \omega_{osc}^2 C_1C_2L \Rightarrow \omega_{osc} = \frac{1}{\sqrt{L\frac{C_1C_2}{C_1+C_2}}}$$

which means that there is a series resonance in the loop (LC_1C_2).

Hartley Oscillator:-



$$\beta = \frac{v_f}{v_o} = \frac{sL_1}{sL_1 + \frac{1}{sC}} = \frac{s^2L_1C}{s^2L_1C + 1}$$

$$A = \frac{v_o}{v_\pi} = \frac{-g_m v_\pi \left(R \,||\, sL_2 \,||\, \left(sL_1 + \frac{1}{sC}\right)\right)}{v_\pi}$$

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after simplification we get

$$AB = -g_m \left(\frac{S^3 R L_1 L_2 C}{S^2(RCL_2 + L_1CR) + R + S^3 L_1 L_2 C + SL_2} \right)$$

$$AB = -g_m \left(\frac{S^2 R L_1 L_2 C}{S(RCL_2 + L_1CR) + \frac{R}{S} + S^2 L_1 L_2 C + L_2} \right)$$

at ω_{osc}, imaginary part = 0 we get:-

$$\omega_{osc} RCL_2 + \omega_{osc} L_1 CR = \frac{R}{\omega_{osc}}$$

$$CL_2 + CL_1 = \frac{1}{\omega_{osc}^2}$$

$$\omega_{osc}^2 = \frac{1}{C(L_2 + L_1)} \Longrightarrow \omega_{osc} = \frac{1}{\sqrt{C(L_2 + L_1)}}$$

also series resonance between them.

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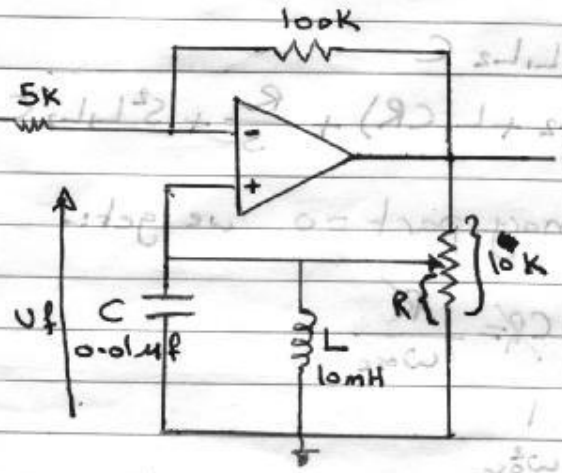
15-19 new Millman

Example: (1) 17.32 (Millman).

For the oscillator shown find the frequency of oscillation, and the minimum value of R.



$$A\beta = \left(1 + \frac{100k}{5K}\right) * \frac{Z}{Z + (10^4 - R)}$$

$$Z = \frac{1}{j\omega C + \frac{1}{j\omega L} + \frac{1}{R}}$$

Substitute Z in the Aβ equation and set the imaginary part to zero to find fosc.

we get :-

$$f_{osc} = \frac{1}{2\pi\sqrt{LC}}$$ which is the resonance frequency for LC.

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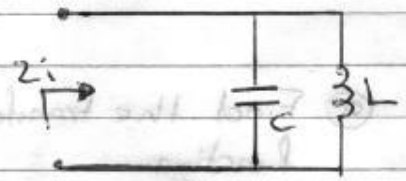

$$Z_{ip} = \frac{j\omega L * \frac{1}{j\omega C}}{j(\omega L - \frac{1}{\omega C})} = \infty$$

at resonance

$$\therefore f_{osc} = \frac{1}{2\pi\sqrt{LC}}$$

$$= \frac{1}{2\pi\sqrt{10 * 10^{-3} * 0.01 * 10^{-6}}} = 15.92\,kHz.$$

$$Z_{is} = j(\omega L - \frac{1}{\omega C}) = 0$$

at resonance.

At f_{osc}, $Z = R$.

$$\beta = \frac{R}{10^4}, \quad A = 1 + \frac{100}{5} = 21$$

$$(21)\left(\frac{R}{10^4}\right) > 1$$

$$R > \frac{10^4}{21} \Rightarrow R > 476\ \Omega$$

$$\therefore R_{min} = 476.$$

(d)

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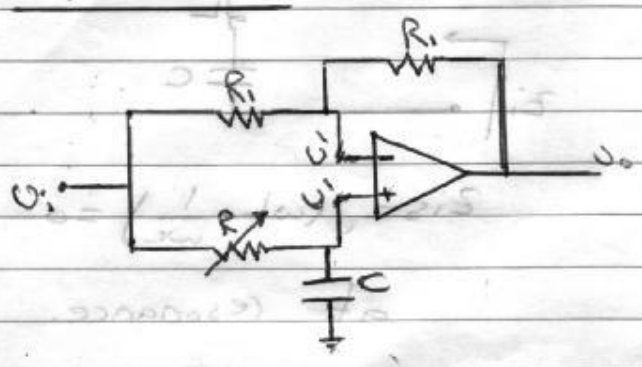
Example:- (17.30) Millman.



(a) Find the transfer function

(b) Find the phase.

tranfer function

$$\frac{v_i - v'}{R_1} = \frac{v' - v_o}{R_1} \quad \text{---(1)}$$

$$v' = v_i \left(\frac{\frac{1}{sc}}{R + \frac{1}{sc}} \right) \quad \text{---(2)}$$

(a) $$\frac{v_o}{v_i} = \frac{1 - sCR}{1 + sCR}$$

$$\frac{v_o}{v_i} = \frac{1 - j\omega CR}{1 + j\omega CR}$$

$\left| \frac{v_o}{v_i} \right| = 1$ always for all frequencies

only the phase changes with frequency.

(b) $\phi = -2\tan^{-1}(\omega CR)$

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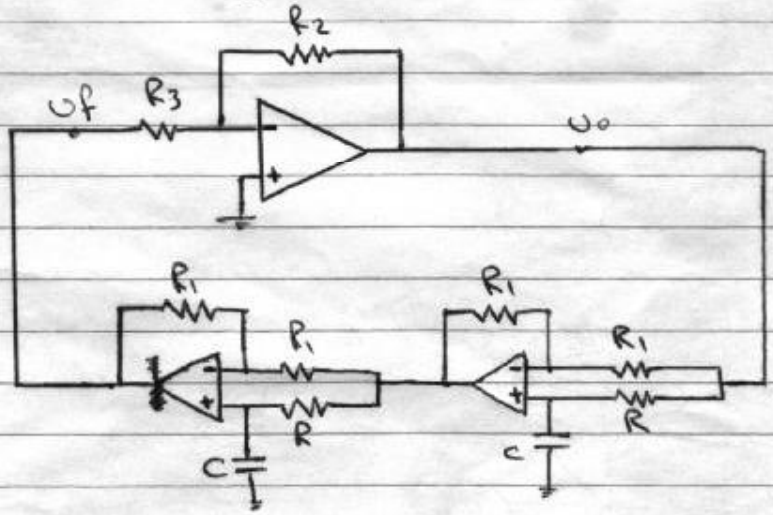
(b) $\phi = -2\tan^{-1} \omega CR$

If R is varied as C remains constant, this configuration acts as a constant-amplitude phase shifter.

If $R=0$, $\phi=0$
If $R=\infty$, $\phi=-180$ or 180

(c) If two phase shifters are cascaded and the loop is completed with an inverting op-amp then this system will oscillate at a frequency f_{osc} as following :-



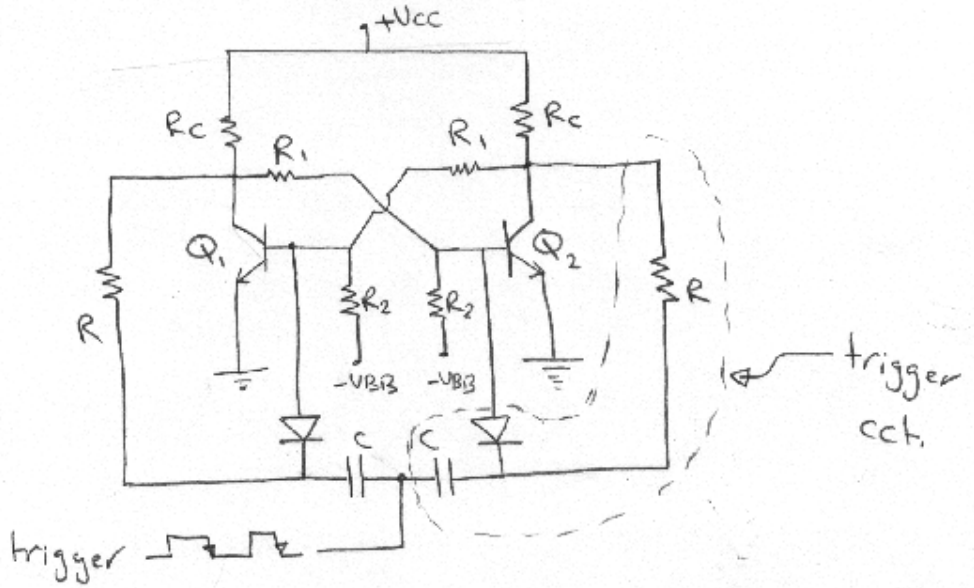
ϕ_T = total phase shift of the β-network only

$\phi_T = -4\tan^{-1} \omega CR$

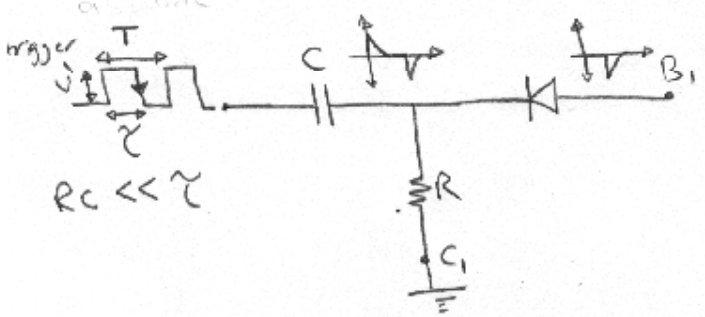
$\phi_T = -180$ at f_{osc}.

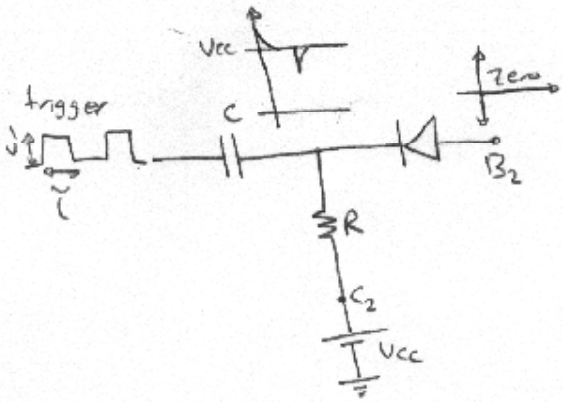
Multivibrators

1) Bistable Multivibrators :-



Assume Q_1 ON and Q_2 off.

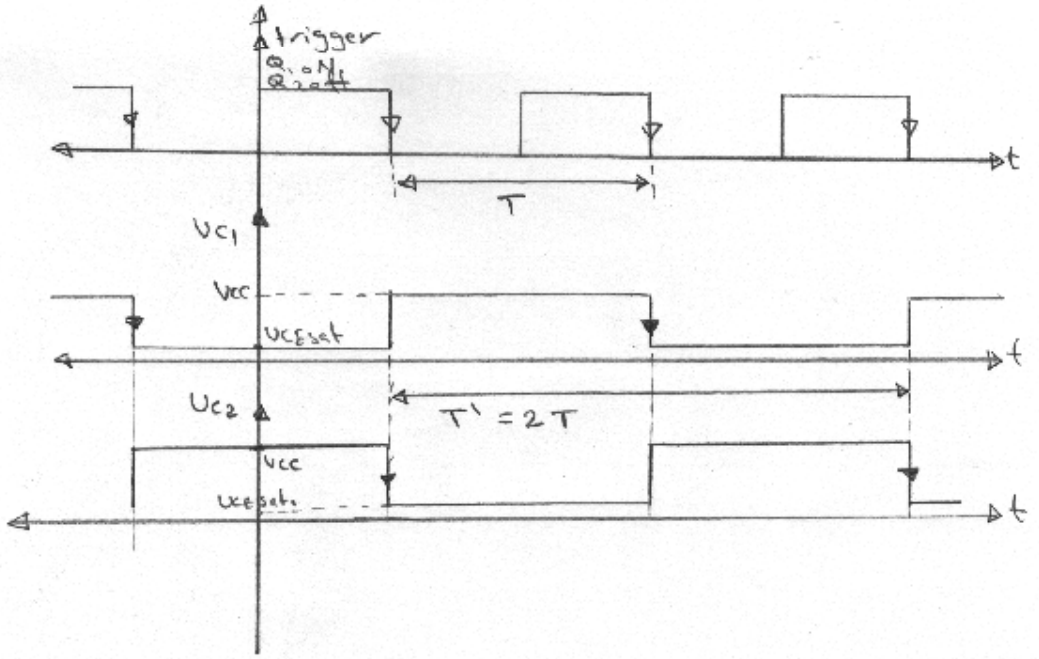


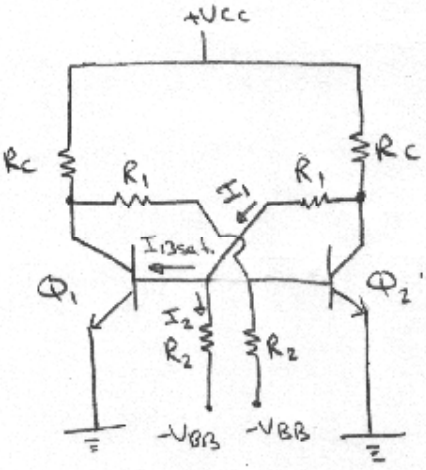


The Bistable multivibrator has two stable states :-

① when Q_1 ON , Q_2 off.

② when Q_1 off , Q_2 ON.





In order to design this circuit, assume on of the transistors are ON and the other off, so let Q_1 ON and Q_2 off.

$$R_c = \frac{V_{cc} - V_{CEsat.}}{I_{csat.}}$$

$$I_1 = I_2 + I_{Bsat.}$$

$$I_1 = \frac{V_{cc} - V_{BE}}{R_c + R_1} = \frac{V_{BB} + V_{BE}}{R_2} + I_{Bsat.} \quad \text{——(1)}$$

$$I_{Bmin} = \frac{I_{csat.}}{\beta}$$

$I_{Bsat.} > I_{Bmin}$ (In order for the transistor Q_1 to be well in saturation)

assume $I_{Bsat.} = 2 * I_{Bmin}$.

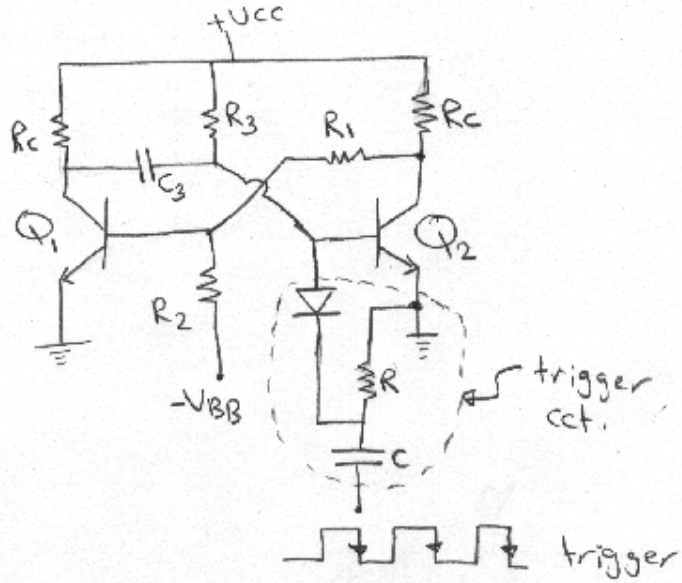
$$V_{B_2} = 0.2 * \frac{R_2}{R_1 + R_2} + (-V_{BB}) \frac{R_1}{R_1 + R_2} \quad \text{—(2)}$$

Assume $V_{B_2} = -1$ (In order for Q_2 to be off).

$$-1 = 0.2 * \frac{R_2}{R_1 + R_2} + (-V_{BB}) \frac{R_1}{R_1 + R_2}$$

This multivibrator is designed such that one transistor is well into saturation and the other is well below cut off.

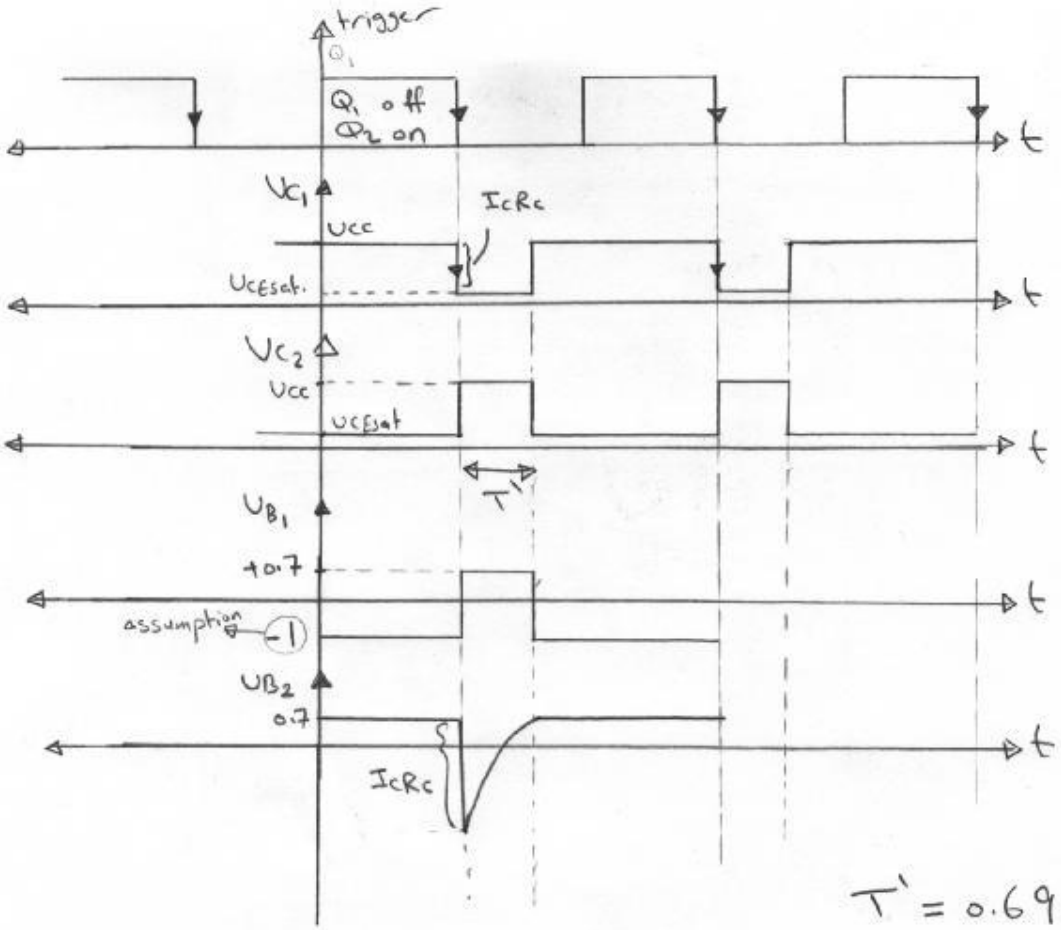
(2) Monostable Multivibrator:-



The monostable multivibrator has one stable and one quasi stable state, they happen when:-

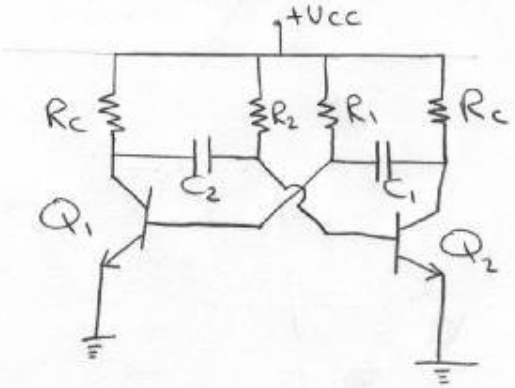
① Q_1 off, Q_2 on (stable).

② Q_1 on, Q_2 off (quasistable).

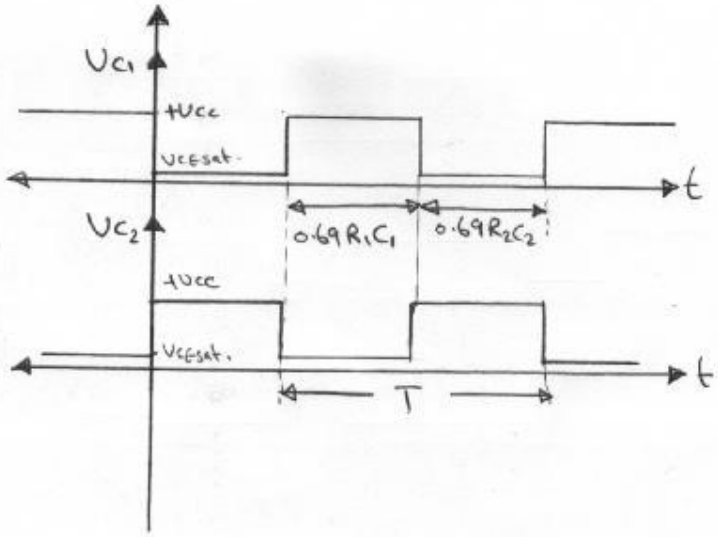


$$T' = 0.69\, R_3 C_3$$

(3) Astable Multivibrator:-



This multivibrator has no stable states. The circuit operates as a free running oscillator without external trigger.



T = period of the pulse train.

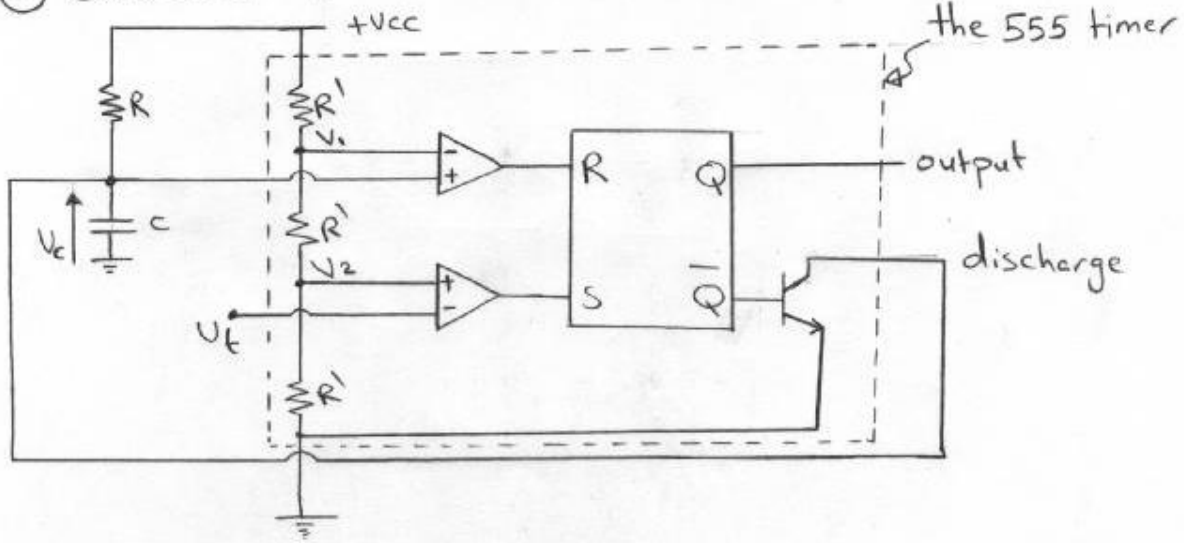
$T = 0.69 R_1C_1 + 0.69 R_2C_2$.

if $R_1 = R_2 = R$ and $C_1 = C_2 = C$

then we have a square waveform generator with a period $T = 1.38\ RC$.

The 555 timer

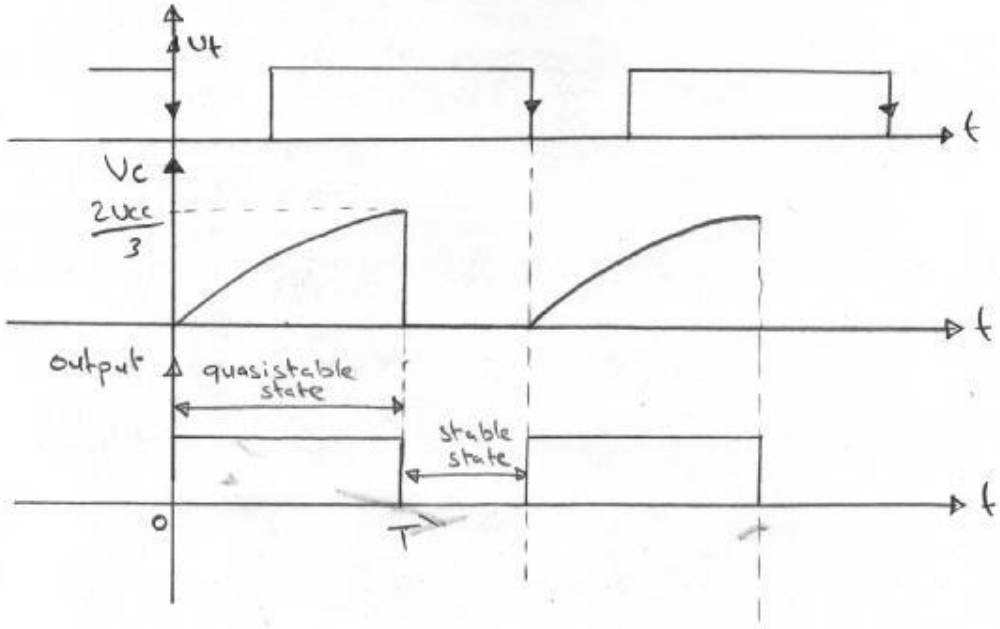
(a) Connected as a monostable cct.:-



$V_1 = \frac{2V_{cc}}{3}$, $V_2 = \frac{V_{cc}}{3}$

V_t :- trigger

$V_t > \frac{V_{cc}}{3}$

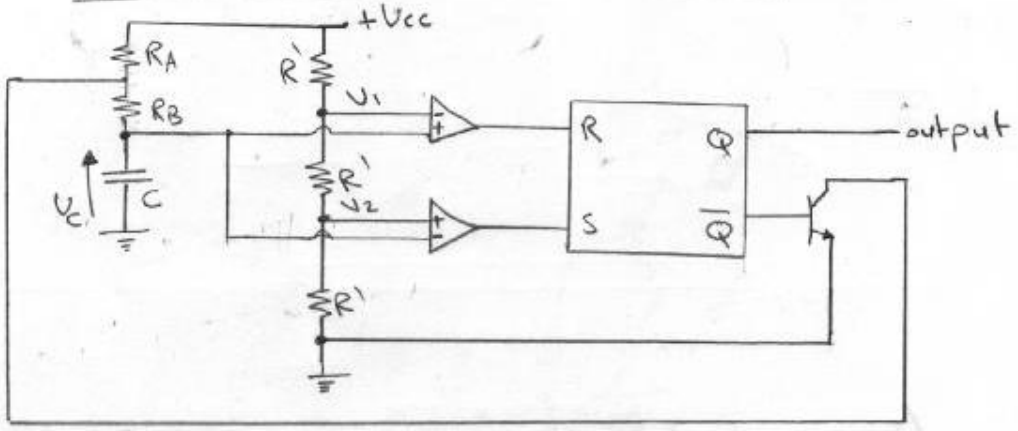


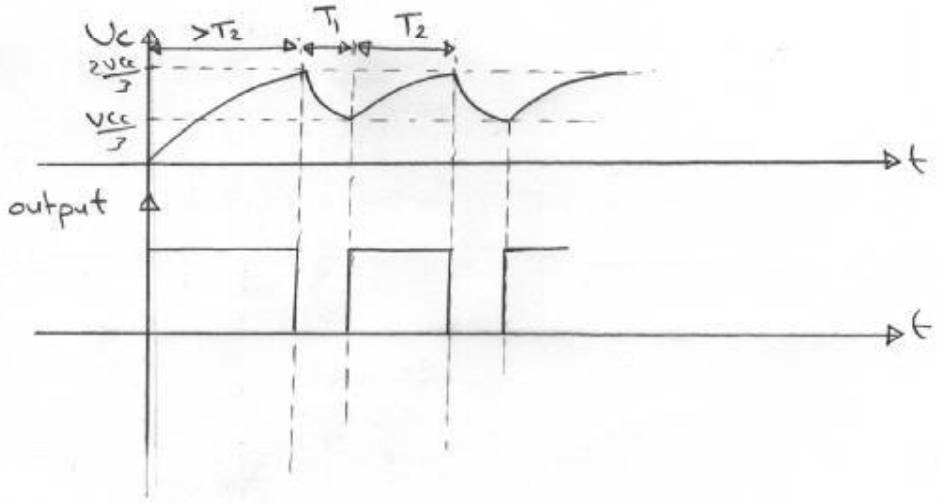
$$V_c = V_{cc}\left(1 - e^{-t/\tau}\right)$$

$$\frac{2V_{cc}}{3} = V_{cc}\left(1 - e^{-T'/RC}\right)$$

$$T' = (\ln 3)\,RC$$

(b) Connected as an astable cct. :-





$T = T_1 + T_2$

$f = \frac{1}{T}$

To find T_1 :-

$$V_c = \frac{2V_{cc}}{3} e^{-t/(R_B C)}$$

$$\frac{V_{cc}}{3} = \frac{2V_{cc}}{3} e^{-T_1/(R_B C)}$$

$$T_1 = [\ln 2] R_B C$$

To find T_2 :-

$$V_c = V_{cc} + \left(\frac{V_{cc}}{3} - V_{cc}\right) e^{-t/[(R_A+R_B)C]}$$

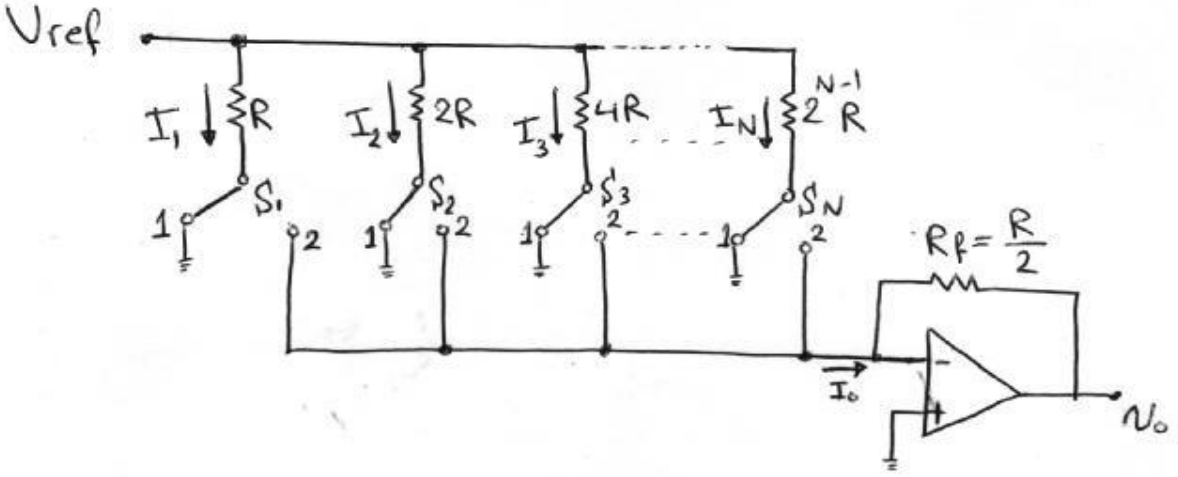
$$\frac{2V_{cc}}{3} = V_{cc} + \left(\frac{V_{cc}}{3} - V_{cc}\right) e^{-T_2/[(R_A+R_B)C]}$$

$$T_2 = [\ln 2] (R_A + R_B) C$$

$$T = (\ln 2) C (2R_B + R_A) \text{ , Duty cycle } = \frac{R_A + R_B}{R_A + 2R_B}$$

Digital-to-Analog (D/A) converters:-

① Binary-weighted Resistor D/A Converter:-



An N-bit D/A converter using binary weighted resistors

* The switches are controlled by an N-bit digital input: $(b_1, b_2, \ldots, b_N)$.
* b_i is either 0 or 1.
* b_N is the least significant bit (LSB) and b_1 is the Most " " (MSB).

* if $b_i = 1$ the switch is at position (2)
  if $b_i = 0$ the switch is at position (1)

$$I_o = I_1 b_1 + I_2 b_2 + I_3 b_3 + \cdots + I_N b_N .$$

$$= \frac{V_{ref}}{R} b_1 + \frac{V_{ref}}{2R} b_2 + \frac{V_{ref}}{4R} b_3 + \cdots + \frac{V_{ref}}{2^{N-1} R} b_N .$$

$$D = \frac{b_1}{2^1} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + \cdots + \frac{b_N}{2^N}$$

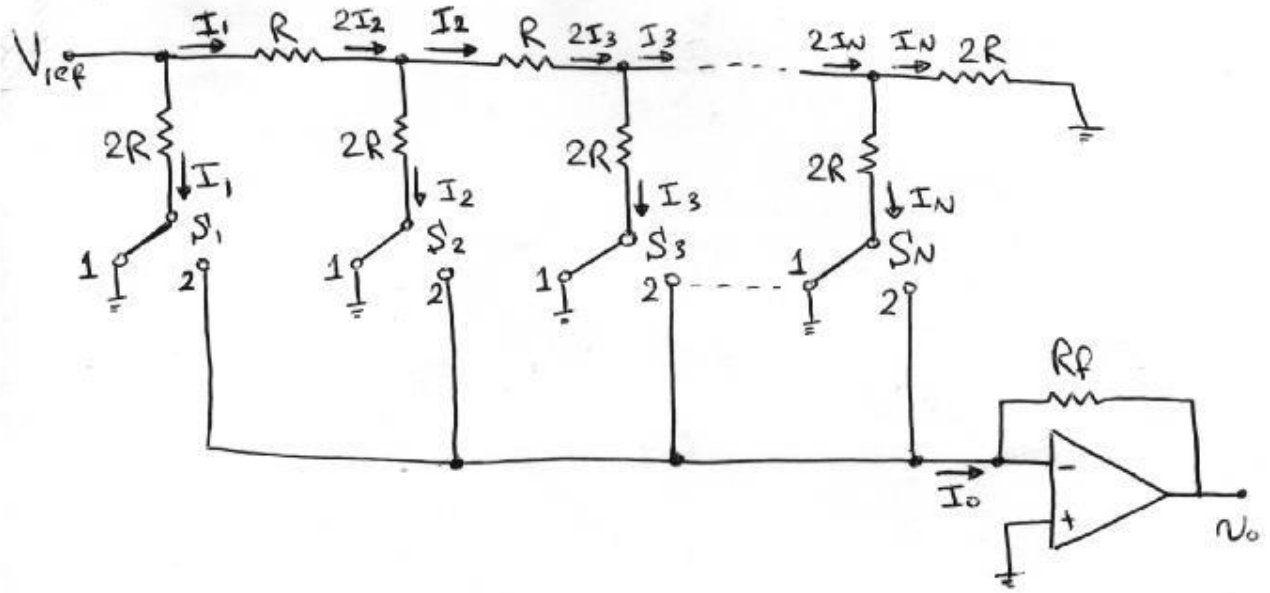
$$I_o = \frac{2V_{ref}}{R} D$$

$$V_o = -I_o R_f = -V_{ref} D .$$

so that the output V_o is directly proportional to the digital input signal.

* a disadvantage of Binary weighted Resistor D/A converter is that when $N > 4$ there will be a difficulty in maintaining accuracy of resistor values.

② The R-2R Ladder D/A



$$I_o = I_1 b_1 + I_2 b_2 + \cdots + I_N b_N$$

$$I_1 = 2I_2 = 4I_3 = \cdots = 2^{N-1} I_N$$

$$I_1 = \frac{V_{ref}}{2R}$$

$$I_o = \frac{V_{ref}}{R}\left(\frac{b_1}{2^1} + \frac{b_2}{2^2} + \cdots + \frac{b_N}{2^N}\right)$$

$$\therefore I_o = \frac{V_{ref}}{R} D$$

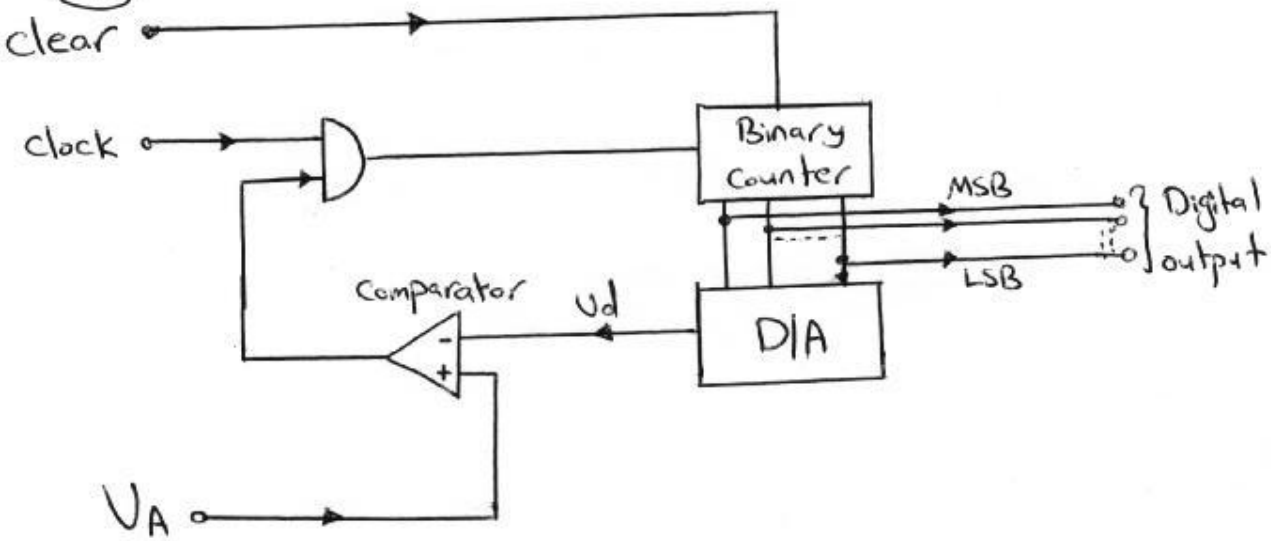
$$V_o = -I_o * R_f$$

$$= -V_{ref} * D \quad \text{if } (R_f = R)$$

Analog-to-Digital (A/D) converters:-

(1) The Counting A/D converter:-

(a)



* The clear pulse resets the counter.
* The counter will then count the number of clock pulses.
* This count will be converted into Analog by (D/A).
* If this count is still less than Va the counter continues untill the counter reaches the value of VA.
* At that point the AND gate is disabled and the counting stops.

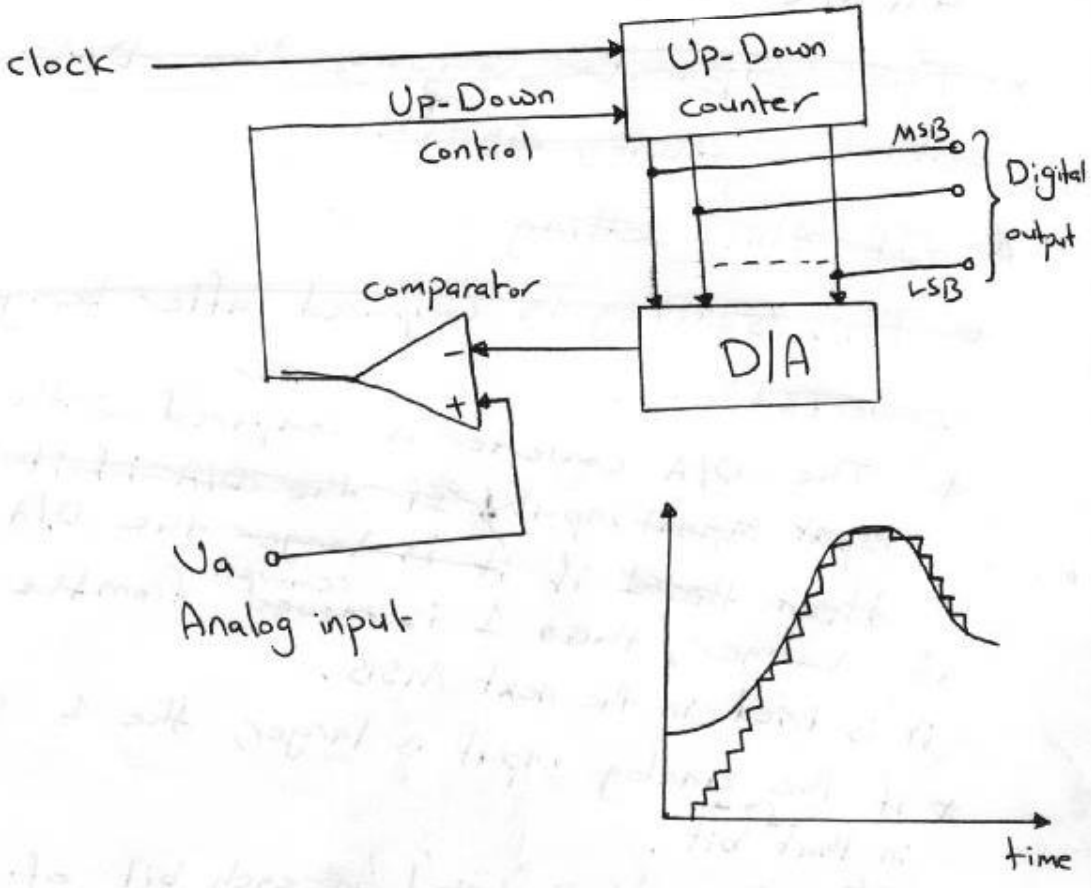
* The counter reading represents the analog input

* If Va is varying with time then a sample and hold circuit is required. The minimum interval between samples is to be nT seconds, where

n = is the number of clock pulses for the maximum value of the analog voltage.

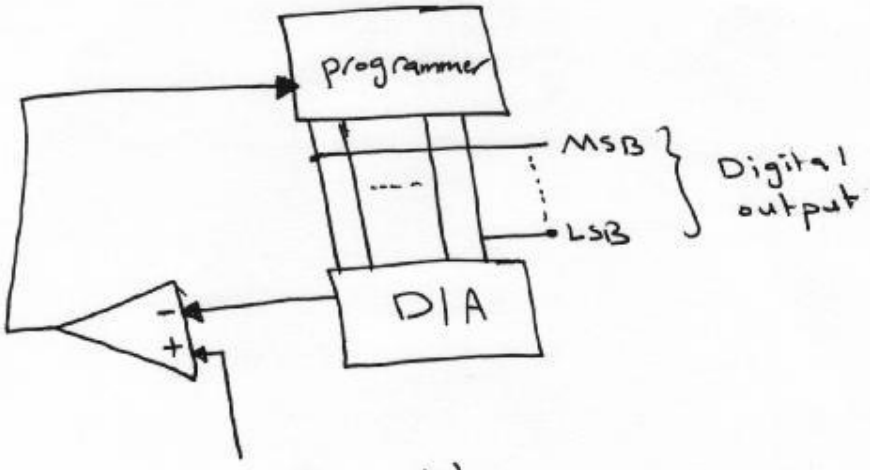
T = is the clock period.

(b) Tracking or Servo counting A/D converter:-



The Conversion time is small for small changes in the sampled analog signal and hence this system can be used effectively as a tracking A/D Converter.

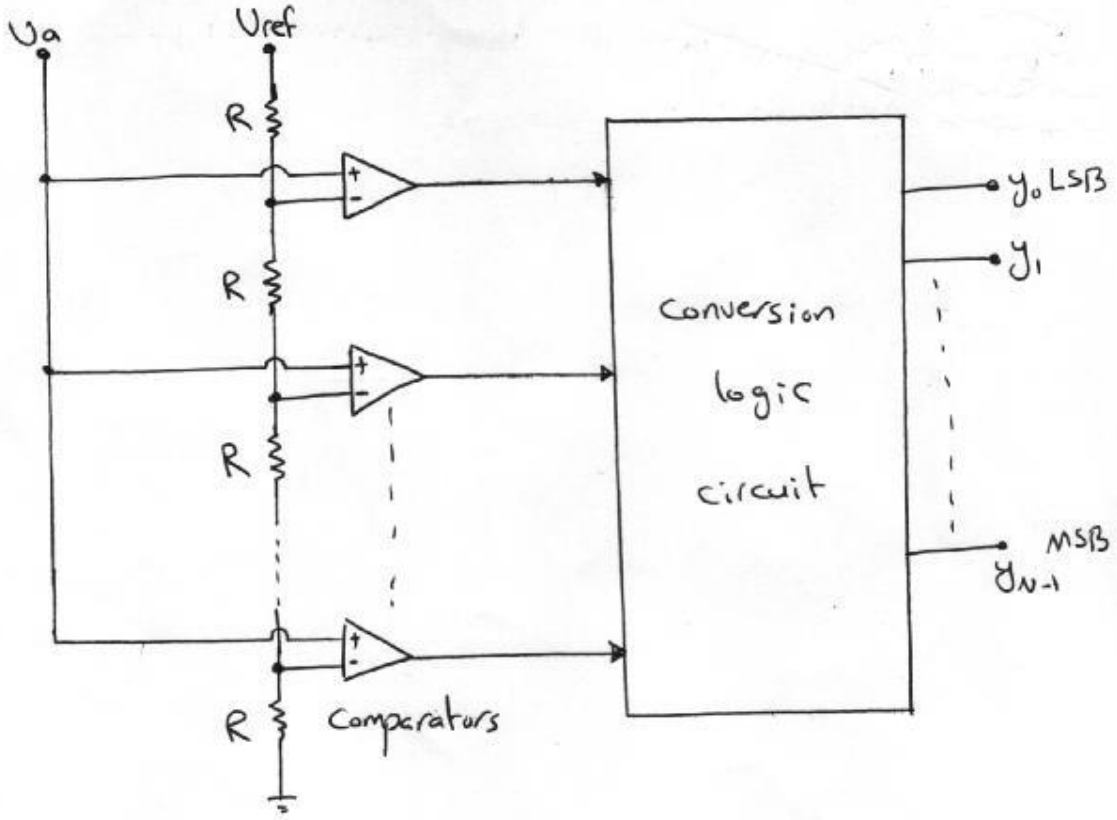
(2) The Successive - Approximation A/D Converter



* The programmer sets the MSB to 1 with all other bits to 0.
* The D/A Converter output is compared with the analog input, if the D/A output is larger, the 1 is removed from the MSB, and it is tried in the next MSB.
* if the analog input is larger, the 1 remains in that b
* Thus a 1 is tried in each bit of the D/A Converter until the binary equivalent of the analog Signal is obtained at the end of the process.

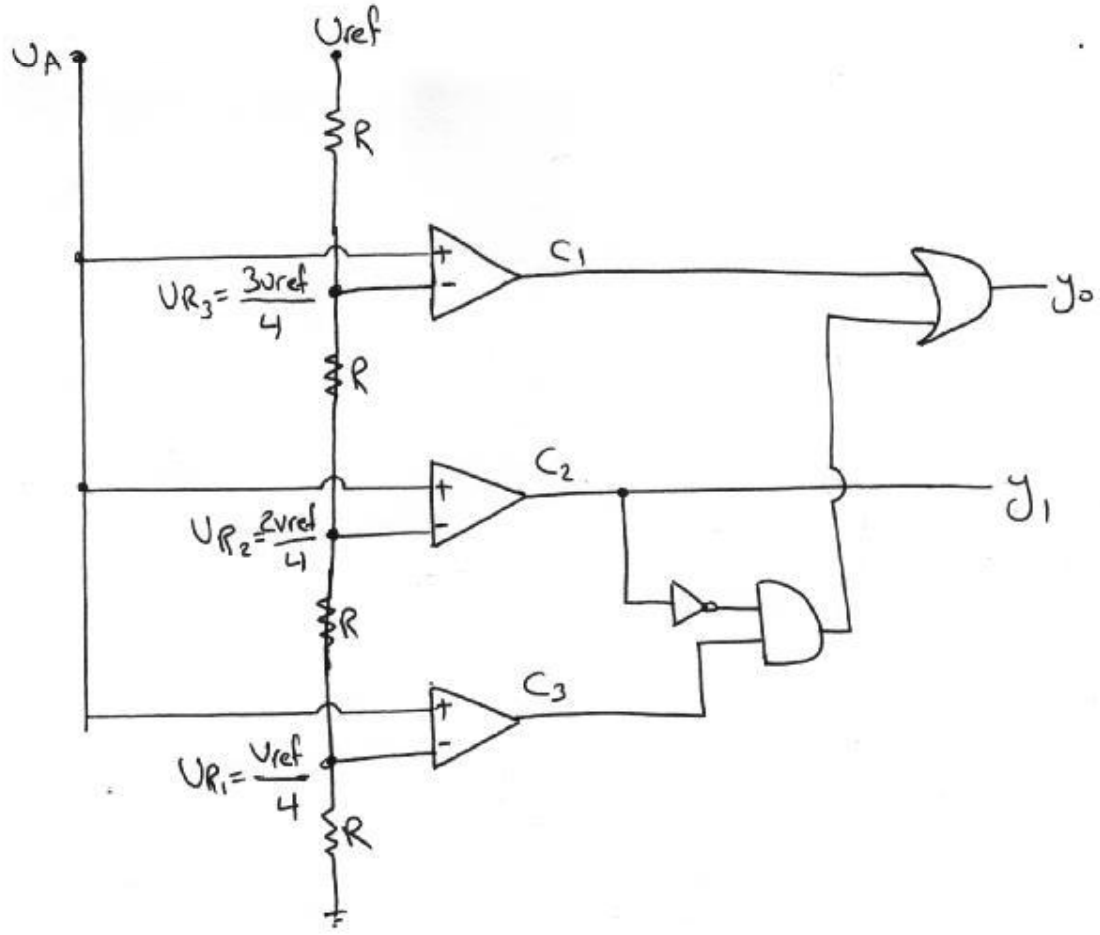
* For an N-bit system, the conversion time is N clock periods as opposed to a worst case of 2^N clock periods for the counting-type A/D converter.

(2) The Simultaneous, parallel or Flash A/D converter :-



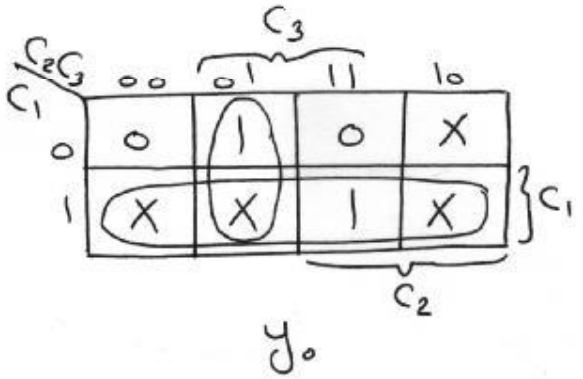
This converter is the fastest of all converters.

for example if $N=2$ then 3 comparators are required where Va is applied to them simultaneously and compared with equally spaced thresholds as in the following:-



* a disadvantage of this technique is the complexity of hardware. The number of comparators needed is $2^N - 1$ where N is number of output bits.

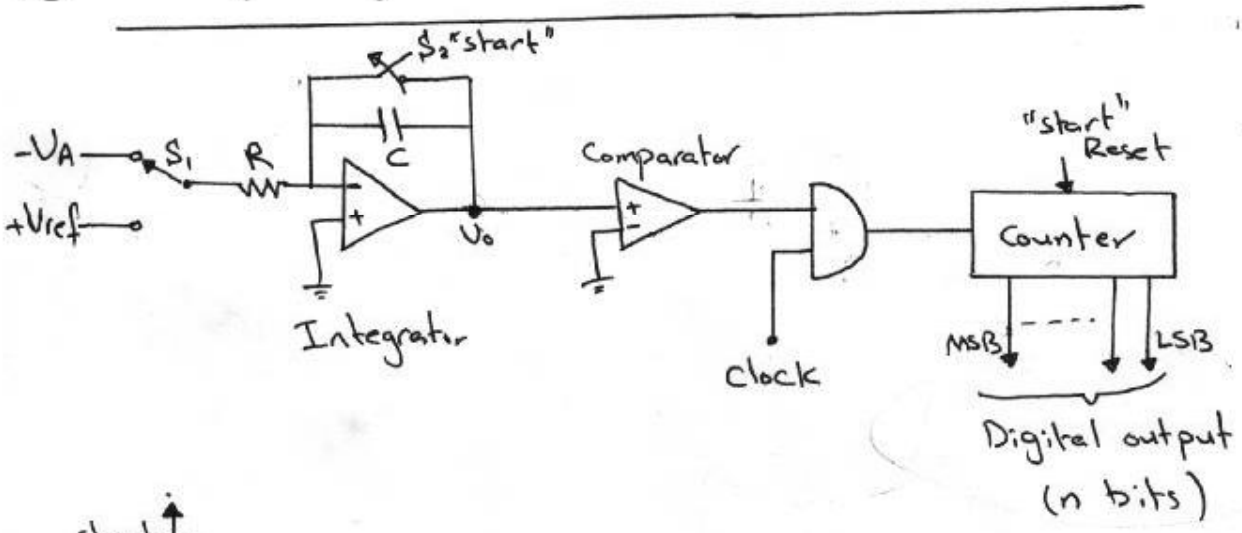
V_a	C_3	C_2	C_1	y_1	y_0
$0 < V_a < \frac{V_{ref}}{4}$	0	0	0	0	0
$\frac{V_{ref}}{4} < V_a < \frac{2V_{ref}}{4}$	1	0	0	0	1
$\frac{2V_{ref}}{4} < V_a < \frac{3V_{ref}}{4}$	1	1	0	1	0
$\frac{3V_{ref}}{4} < V_a < V_{ref}$	1	1	1	1	1

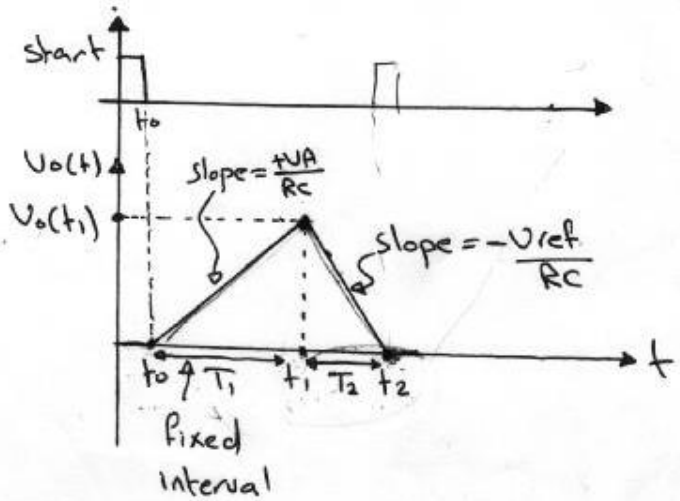


$$Y_1 = C_2$$

$$Y_0 = C_1 + C_3\overline{C_2}$$

(14) Integrating Dual-Slope A/D Converter:-





$$V_o(t_1) = \frac{-1}{RC}\int_{t_0}^{t_1} (-V_A)\, dt = \frac{V_A}{RC}(t_1 - t_0)$$

$N_1 = 2^n$

$T_1 = (t_1 - t_0) = N_1 T$, T = clock period.

$f_c = \frac{1}{T}$, f_c: clock frequency

$$\therefore V_o(t_1) = \frac{V_A}{RC} \cdot N_1 T$$

$$V_o(t_2) = V_o(t_1) + \frac{-1}{RC}\int_{t_1}^{t_2} V_{ref}\, dt$$

$$0 = V_o(t_1) + \frac{-1}{RC}\int_{t_1}^{t_2} V_{ref}\, dt .$$

$$\frac{V_A}{RC} \cdot N_1 T = \frac{V_{ref}}{RC}(t_2 - t_1)$$

$$T_2 = t_2 - t_1 = N_2 T$$

$$\therefore \frac{V_A}{RC} \cdot N_1 T = \frac{V_{ref}}{RC} \cdot N_2 T$$

$$N_2 = \frac{N_1}{V_{ref}} V_A$$

$$\boxed{N_2 = K(V_A)} \text{ , where } K = \frac{N_1}{V_{ref}}$$

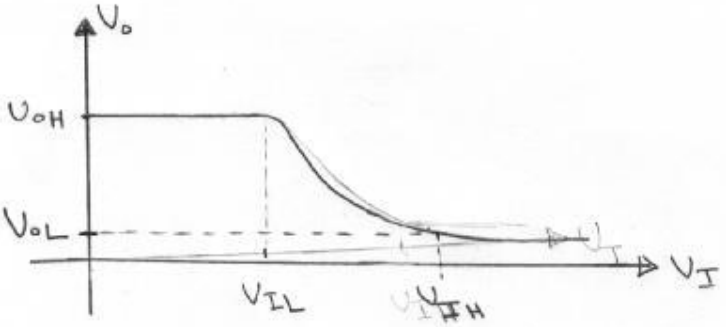
This converter is very accurate but very slow.

Logic families

Logic circuit characterization:-

The following parameters are used to characterize the operation and performance of a logic-circuit family.

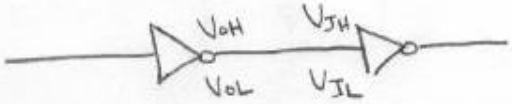
(a) Noise Margins:-



Typical voltage transfer c/c's (VTC) of a logic inverter

* The V_{IL} is the maximum value that the input can have while being interpreted by the inverter as representing a logic (0).
* The V_{IH} is the maximum value that V_I can have while being interpreted by the inverter as representing logic (1).

for example:-



$N_{MH} = V_{OH} - V_{IH}$

$N_{ML} = V_{IL} - V_{OL}$

* The robustness of the logic cct. family is defined by its ability to reject noise and thus by its noise margins (NM_H , NM_L).

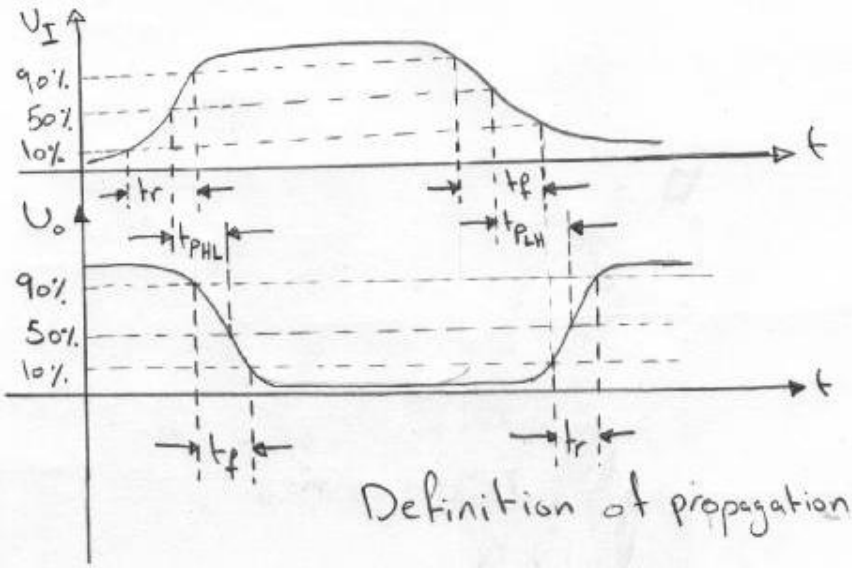
(b) power dissipation

There are two types of power in a logic gate, static and Dynamic.

static power dissipation :- is the power the gate dissipate in the absence of switching action. It results from the presence of a path between the power supply and ground in one or both of its two state. (i.e. with the o/p either low or high).

Dynamic power dissipation :- Occures only when the gate is switched due to the presence of a capacitor between the o/p node and ground.

(c) propagation delay :-



Definition of propagation delay

t_r : the rise time.

t_f :- the fall time.

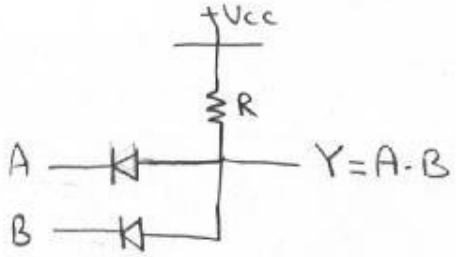
t_{PHL} :- High-to-Low propagation delay.

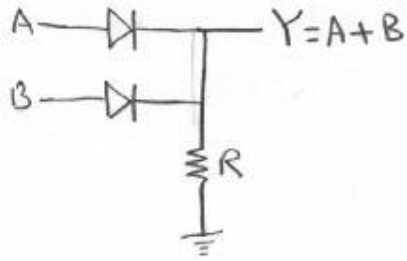
t_{PLH} :- Low-to-High propagation delay.

(d) Fan out:-

The fan out is the maximum number of similar gates that a gate can drive while remaining within gauranteed specifications.

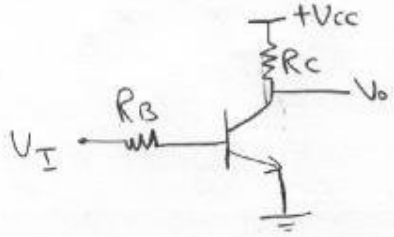
(1) Diode Logic family





The BJT Digital Circuits:-

Basic BJT Inverter:-



Example:-

Draw the VTC of the basic BJT inverter if $R_B = 10K\Omega$, $R_C = 1K\Omega$, $\beta_F = 50$ and $V_{CC} = 5V$.

Solution:-

(1) if the i/p equals a low voltage

$V_I = V_{oL} = V(o) = 0.2V = V_{CEsat.}$

$V_o = V_{oH} = V_{CC} = 5V.$

(2) At $V_I = V_{IL}$, the transistor begins to turn on, then

$V_{IL} = 0.7V.$

(3) if $V_{IL} < V_I < V_{IH}$

the transistor is in the active region having again of

$$A_V = \frac{-\beta_o R_C}{R_B + r_\pi}$$

(4) $$I_{Bmin} = \frac{I_{csat.}}{\beta_F}$$

$$I_{csat.} = \frac{V_{CC} - V_{CEsat.}}{R_C}$$

$V_{IH} = I_{Bmin} * R_B + 0.7 \Rightarrow$ from the i/p loop.

$= 1.66V$

(5) $V_I = V_{oH} = V_{CC} = 5V$

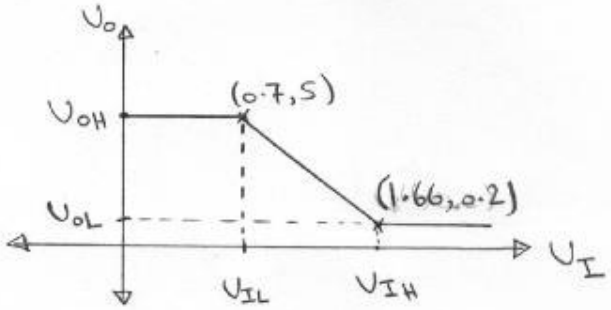
$$I_{csat.} = \frac{V_{CC} - V_{CEsat.}}{R_C}$$

$$I_{Bsat.} = \frac{V_{oH} - 0.7}{R_B}$$

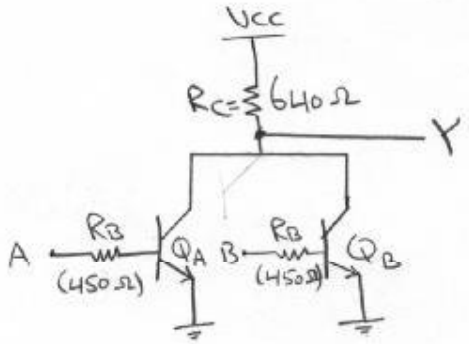
$$\beta forced = \frac{I_{csat.}}{I_{Bsat.}} = 1.1$$

(6) $N_{MH} = V_{OH} - V_{IH} = 3.34\,V$

$N_{ML} = V_{IL} - V_{OL} = 0.5\,V.$



Resistor Transistor Logic (RTL)



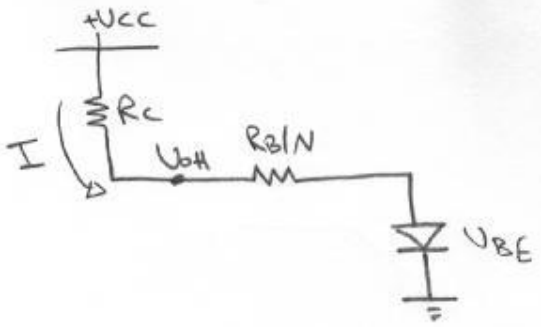
A two input NOR gate of the RTL family

$Y = \bar{A} \cdot \bar{B} = \overline{A+B}$

* The noise margins of the RTL gate are narrow because the V_{OH} is lowered when driving other similar gates.
* The RTL gate dissipate a large amount of power (12 mw).

Example:- An RTL gate is driving N similar gates, find an expression for V_{OH} in terms of N and then find the value of V_{OH}, if N=5.

Solution:-

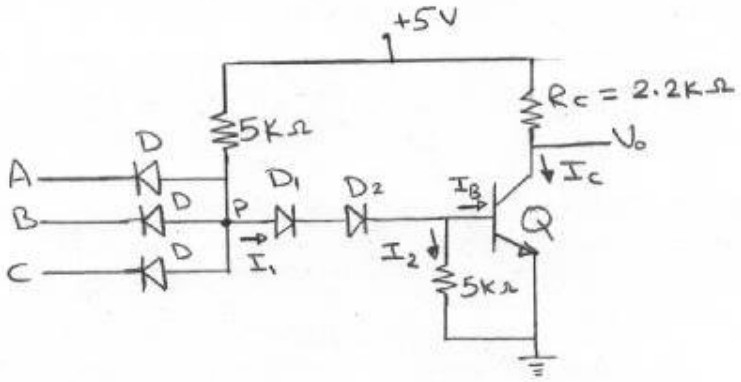


$$V_{oH} = V_{cc} - R_c \frac{V_{cc} - V_{BE}}{R_c + \frac{R_B}{N}}$$

if $V_{cc} = 3V$, $N = 5$

$V_{oH} = \underline{1V}$

Diode Transistor Logic (DTL) family:-



DTL NAND gate

Example:-

For the DTL NAND gate above, assume that $V_{BEsat} = 0.7V$, $V_\gamma = 0.5V$, and $V_{CEsat.} = 0.2V$. The drop across a conducting diode is 0.7V and V_γ(diode) = 0.6V (A) Verify that the cct. functions as a NAND gate for $B_F > B_{Fmin}$ (assume that Q is unloaded by a following gate).

(B) Calculate β_{fmin}.

(C) Will the circuit operate properly if D_2 is not used.

Solution:-

logic (0) = V_{CEsat} = 0.2V.

logic (1) = V_{cc} = 5V.

(A)

* if at least one input is low its diode conducts and V_p = 0.2 + 0.7 = 0.9 V. D_1 and D_2 are not conducting since 3*0.7 = 2.1 V is required and V_{BE} = 0V.

Since V_δ of Q = 0.5 V then Q is off :-

∴ Y = V_{cc} = 5 V = logic (1).

* Now, if all inputs are high at V(1) = V_{cc} = 5V. Assume all input diodes are off, that D_1 and D_2 conduct and that Q is in saturation.

So V_p = 0.7 + 0.7 + 0.7 = 2.1V.

then each input diode (D) will have a voltage of 2.1V on its anode and 5V on its cathode, thus justifying the assumption that D is off.

$$I_1 = \frac{5 - 2.1}{5k} = 0.58 mA.$$

$$I_2 = \frac{0.7}{5k} = 0.14 mA.$$

$$I_B = I_1 - I_2 = 0.44 mA.$$

Assuming that $\beta_F > \beta_{Fmin}$, this value of I_B saturates Q and makes $V_o = V(0) = V_{CEsat}$. So we have verified the NAND gate.

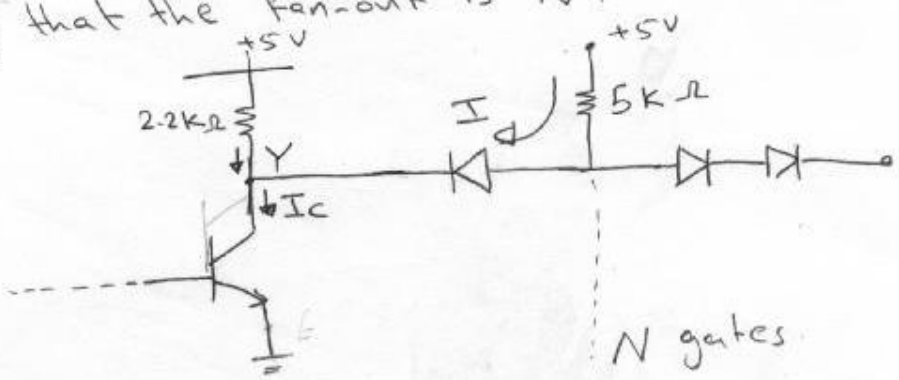
(b) $I_{csat.} = \frac{5 - 0.2}{2.2} = 2.182\,mA$

$\beta_{f\,min} = \frac{I_{csat.}}{I_B} = \frac{2.182}{0.44} = 4.96$

Thus for $\beta_F \geq 4.96$, the assumption of Q is saturated is valid.

(c) If at least one input is at V(0), then $V_p = 0.2 + 0.7 = 0.9V$. Hence if only one diode D_1 is used between p and the base B, then $V_{BE} = 0.9 - 0.6 = 0.3V$, where 0.6V is the diode cut-in voltage. Since the transistor cut-in voltage is $V_\gamma = 0.5V$, theoretically Q is cut-off. However, this is not a very conservative design because a small (>0.2V) spike of noise will turn Q on.

If the DTL gate is driving N similar gates, we say that the fan-out is N :-



when $Y = V(o) = 0.2V$, the input current I. of a following stage adds to the collector current of Q.

Assume all the inputs to the diodes of the following stages are high except the ones driven by Q.

then $I = \frac{5-0.9}{5} = 0.82mA$.

total I_C of $Q = 0.82 \cdot N + 2.182\,mA$.

I_B the same as before loading $= 0.44mA$ and assume a reasonable value of $\beta_{min} = 30$

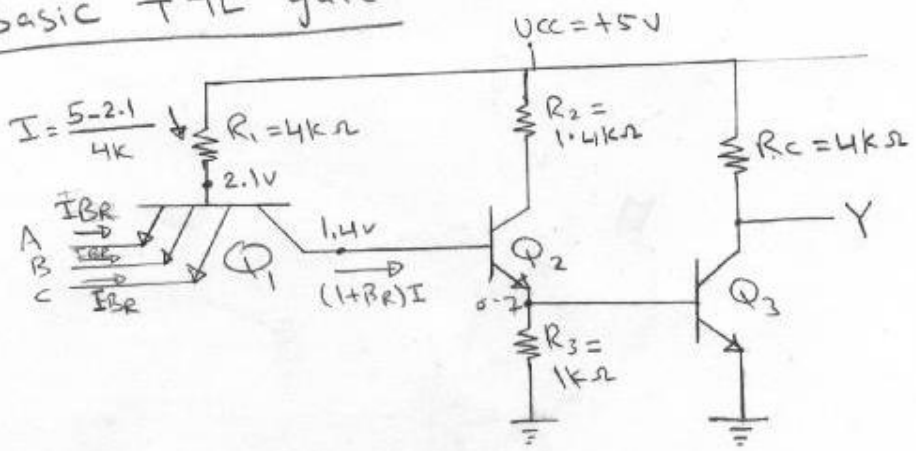
$I_C = \beta_{f\,min}\, I_B$

$I_C = 0.82N + 2.182 = 30 * 0.44 = 13.2mA$.

$N = 13.436$, N must be an integer then $N = 13$. of course the current rating of Q must not be exceeded.

Transistor - Transistor Logic (TTL, T^2L):-

(a) Basic TTL gate:-

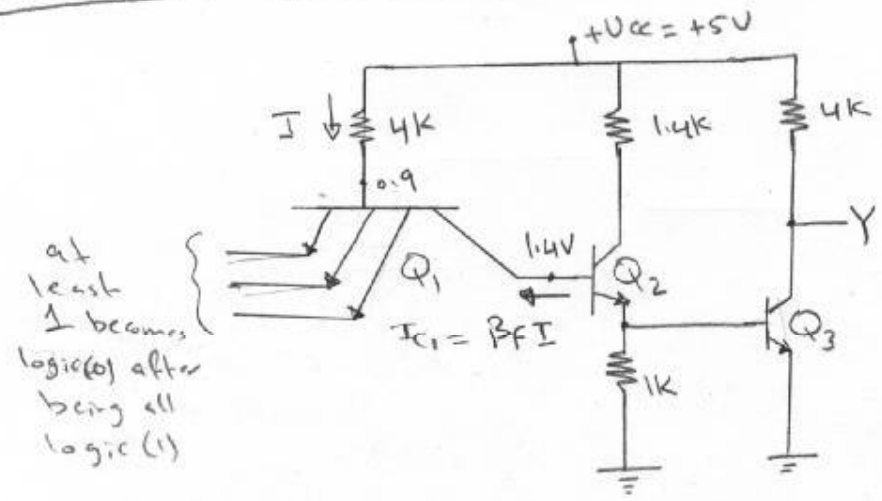


TTL - NAND gate (when all inputs are high)

Case I :- when all inputs are high = logic (1)

* The emitters of Q_1 are reverse biased.
* The collector/Base junction of Q_1 is forward biased.
* Q_1 is operating in the inverted active mode.
* β_R (reverse β) is very small. ($\beta_R = 0.2$)
* $(\beta_R + 1) I$ is a sufficient current to drive Q_2 and Q_3 into saturation and the output Y equals to logic (0) = 0.2V.

Case II :- If at least one of the inputs is V (0).



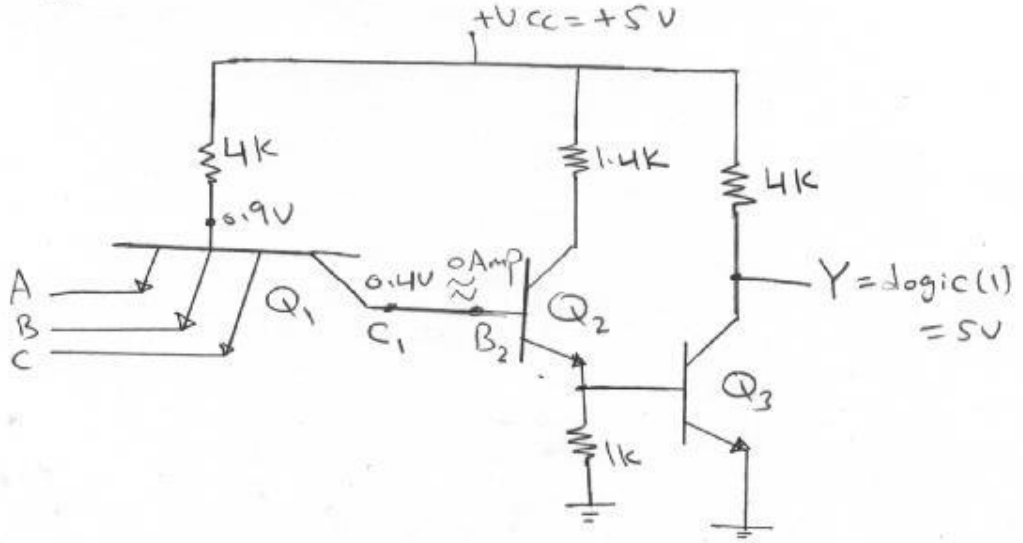
when Q_2 and Q_3 are still momentarily ON (saturated).

* The current I will be diverted to the emitters of Q_1.
* The base/emitter junction of Q_1 is forward biased.
* V_B of Q_1 = 0.9V.
* Q_1 is operating momentarily in the normal active mode.
* $I_{C_1} = \beta_F I$ which is a large current. that will turn Q_2 and Q_3 off.

* when Q_2 is off I_{B_2} is a small current (in nanoamperes), so $I_{B_1} > \frac{I_{C_1}}{\beta}$ and Q_1 will saturate.

* V_{C_1} equals $0.2 + 0.2 = 0.4V$, which is a small voltage that will keep Q_2 and Q_3 off.

$Y = \text{logic}(1) = V_{cc} = 5V$.



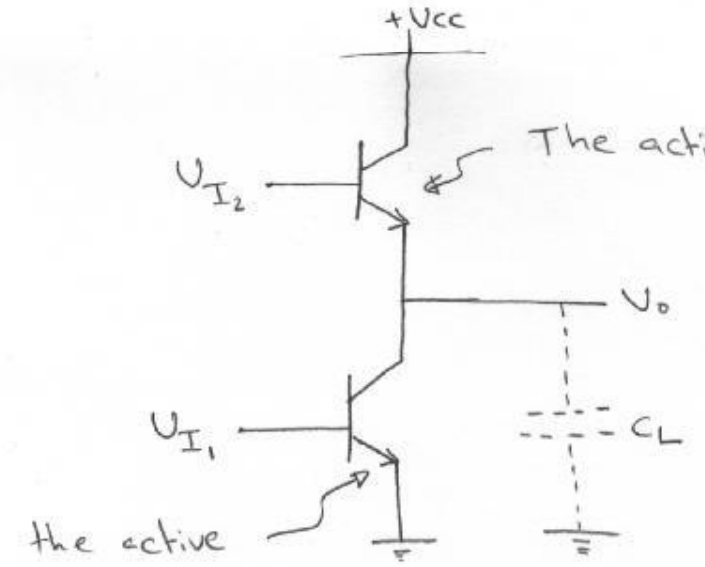
when Q_2 and Q_3 are off.

Output Circuit of TTL:-

* The C.E o/p stage provides fast discharging of a load capacitance but rather slow charging.

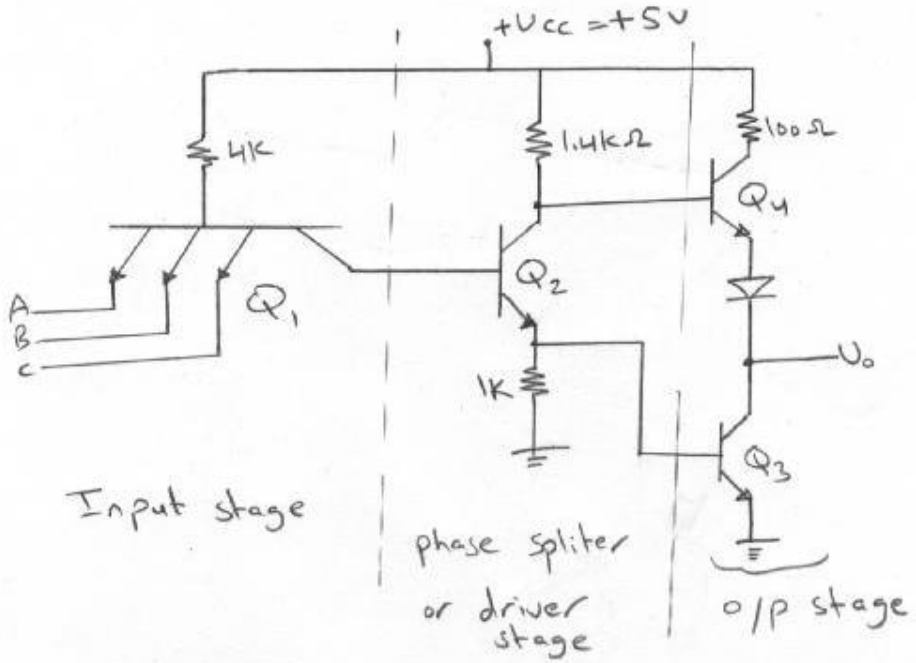
* while the opposite is obtained in the C.C output stage, it provides fast charging of the load capacitance, but slow discharge of C_L.

An optimum output stage will be the totem-pole output stage as shown:-

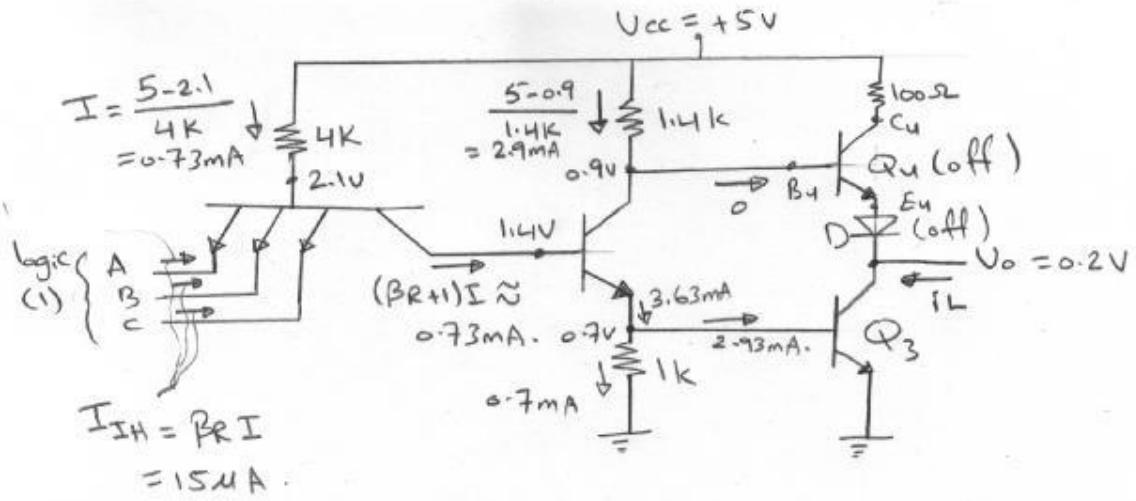


V_{I_1} and V_{I_2} are complementary inputs.

(b) TTL with totem-pole output:-



Case I:- when all inputs are high



* when the input is high both Q_2 and Q_3 are driven into saturation, so $V_o = V_{CEsat.} = 0.2V$.

Q_4 should be off which is obtained by adding Diode D.

* if D does not exist then:-

$$V_{C_2} = V_{CE_{2\,sat.}} + V_{BE_{3\,sat.}} = 0.2 + 0.7 = 0.9\,V.$$

$$V_{BE_4} = V_{B_4} - V_{CE_{3sat.}} = 0.9 - 0.2 = 0.7\,V.$$

which will turn Q_4 ON. and

$$I_{C_4} = \frac{V_{cc} - V_{CE_4(sat.)} - V_{CE_3(sat.)}}{100} = \frac{5 - 0.2 - 0.2}{100}$$

$= 46mA$ (excessive and wasted current).

therefore D was added so that

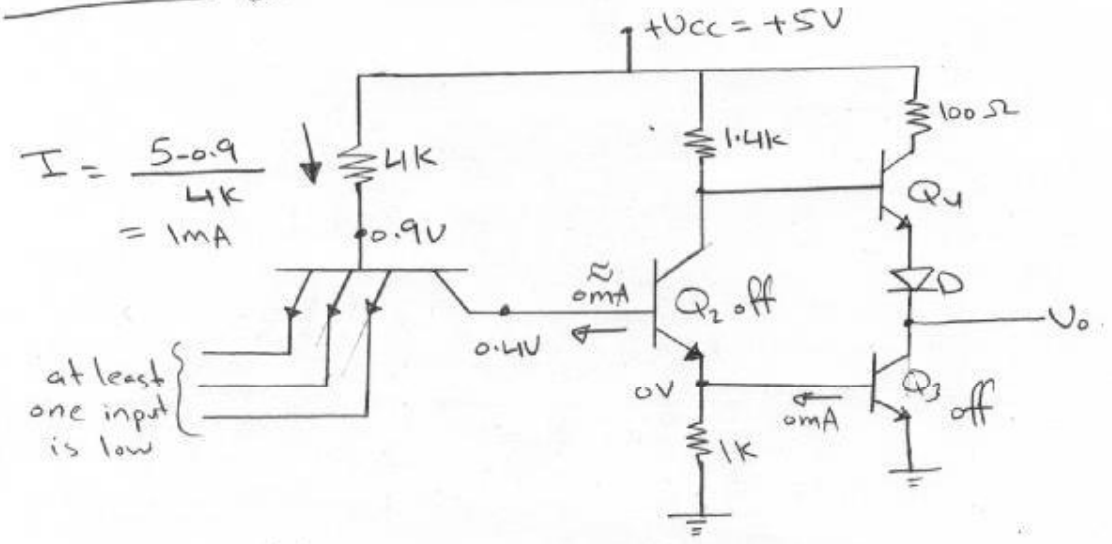
$$V_D + V_{BE_4} = V_{B_4} - V_{CE_3 sat.} = 0.7\,V$$

$\therefore$ Q_4 and D are off since both of them require

1.4V to start conducting.

* In the low output state, the gate can sink a load current (i_L), provided that the value of i_L doesn't exceed $\beta * 2.93mA$ which is the maximum collector current that Q_3 can sustain while remaining in saturation.

Case II when at least one input is low.



Assume that V_o = logic(0) = 0.2V and one of the inputs becomes low.

V_o across C_L (load capacitance) remains momentarily at 0.2V.

Now Q_4 is in saturation and D is conducting,

$$V_{B4} = V_{BE4(sat.)} + V_D + V_o = 0.7 + 0.7 + 0.2 = 1.6V.$$

$$I_{B4} = \frac{V_{cc} - V_{B4}}{1.4K} = \frac{5 - 1.6}{1.4K} = 2.43mA$$

$$I_{C4} = \frac{V_{CC} - V_{CE4} - V_D - V_o}{0.1k} = \frac{5 - 0.2 - 0.7 - 0.2}{0.1} = 39mA$$

$$\beta_{fmin} = \frac{I_{C4}}{I_{B4}} = 16.05$$

Choose $\beta_F > 16.05$ then Q_4 is in saturation. As long as Q_4 is in saturation, the output voltage rises exponentially towards V_{CC} with a very small time constant. The final value of the output voltage is :-

$$V_o = V_{CC} - V_{BE4}(cut in) - V_D(cut in)$$
$$= 5 - 0.5 - 0.6 = 3.9v := logic(1)$$

TTL family with improved performance:-

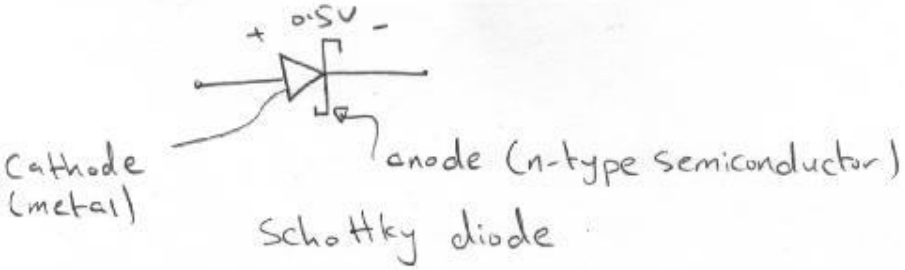
The TTL family is available in series emphasizing either high speed, low power, or both. These gates differ from one another in the numerical values of their resistors and in that some use Schottky transistors.

TTL series

Symbol	meaning
S	Schottky, high speed
LS	schottky, low power
—	standard (the previous one which have been studied)

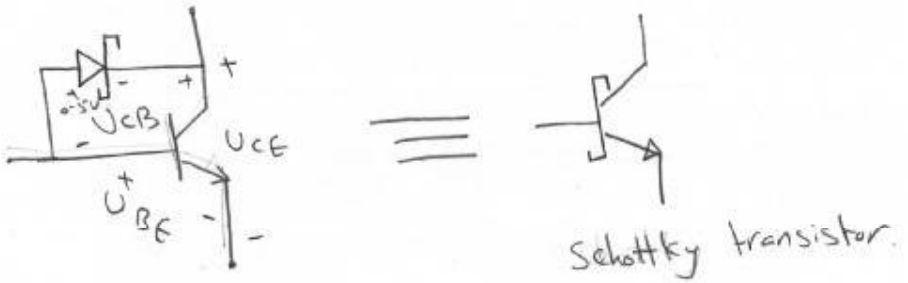
There is the 74 series (0–70°C) and the 54 series (-55 – 125°C).

Schottky TTL (74S)%-



Schottky diode

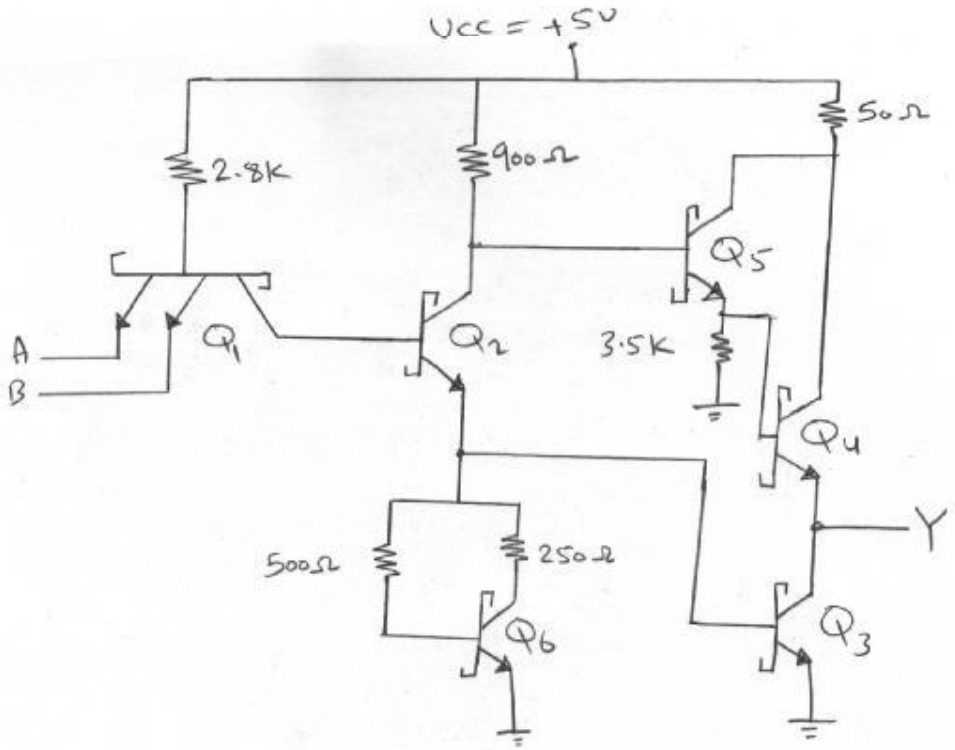
* The schottky diode is formed by bringing metal into contact with a moderately doped n-type semiconductor material.
* The forward voltage drop of the schottky diiode is 0.5V.



Schottky transistor

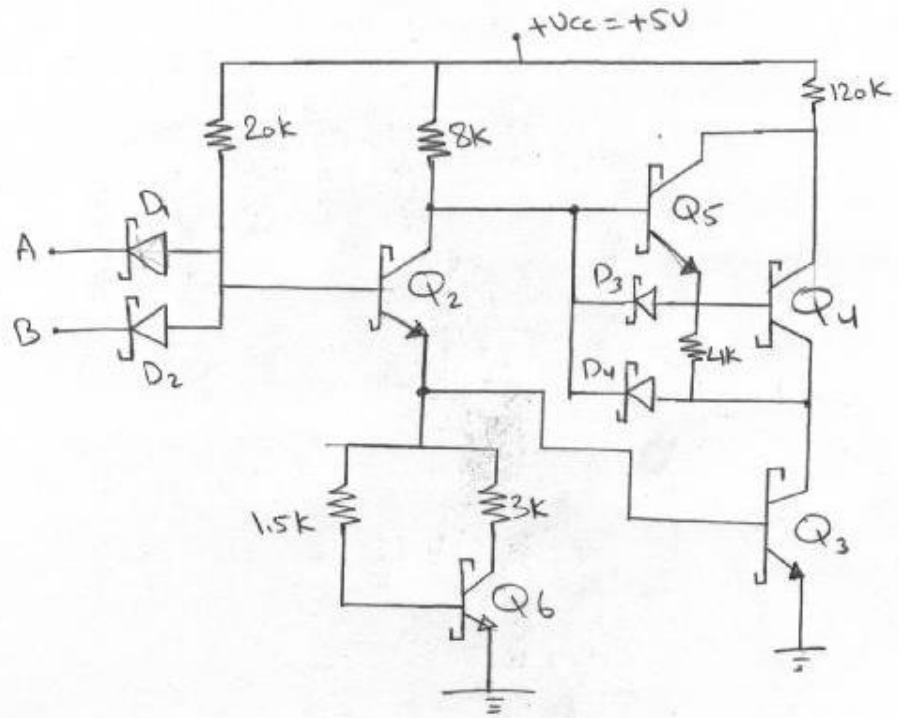
$V_{CE} = 0.7 - 0.5 = 0.2V$

* In schottky TTL, transistors are prevented from saturation by connecting a schottky diode between base and collector of the transistor as shown above.
* By avoiding saturation, the schottky transistor exhibits a very short turn off time.



Schottky TTL NAND gate.

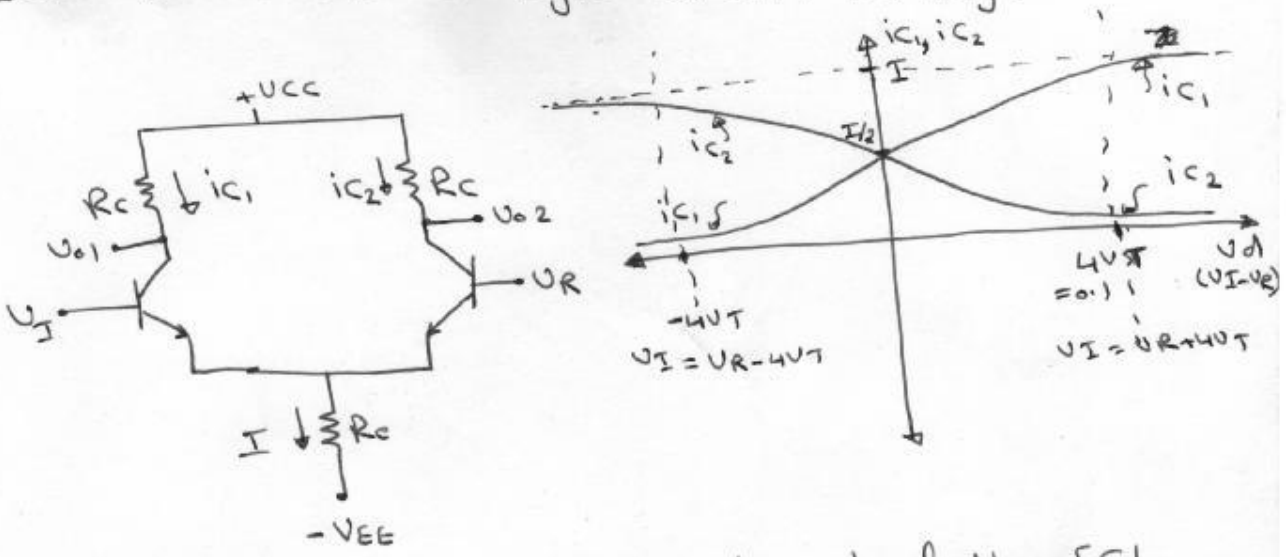
Low power schottky TTL (74LS)



A low-power schottky TTL (LSTTL) gate

Emitter-coupled Logic (ECL)

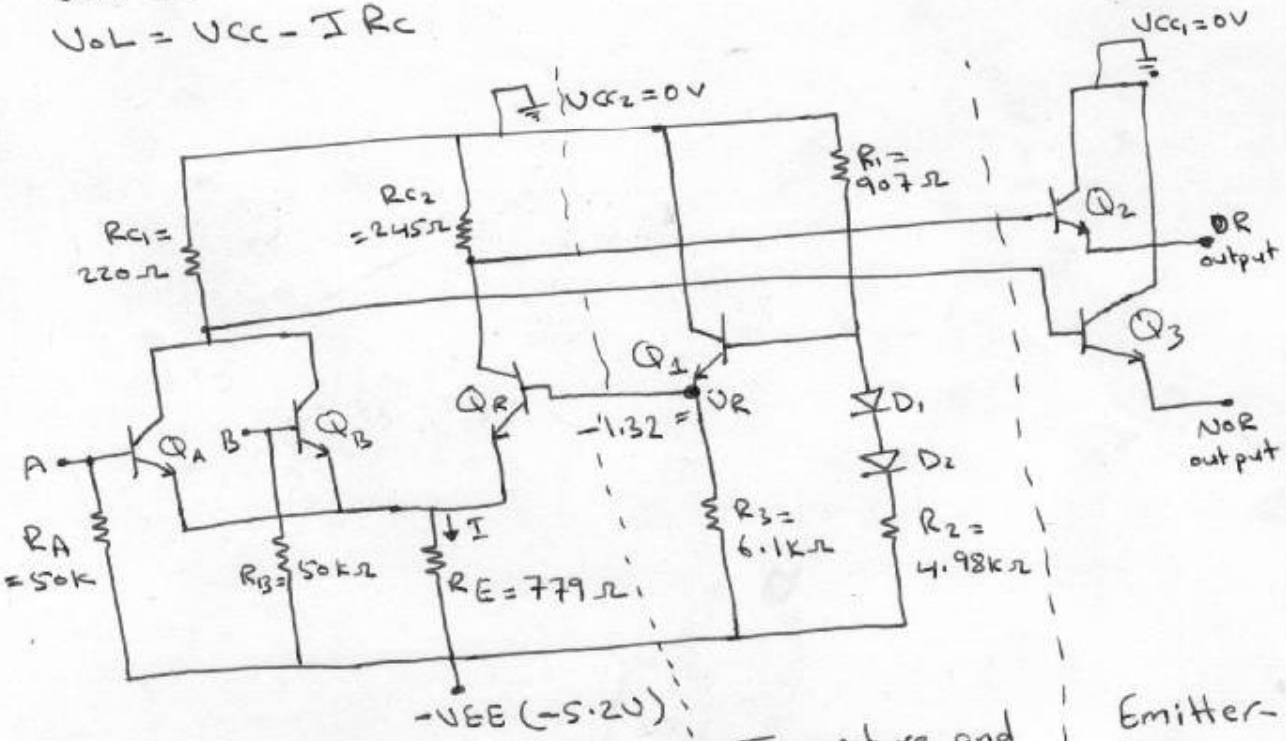
ECL is the fastest logic circuit family.



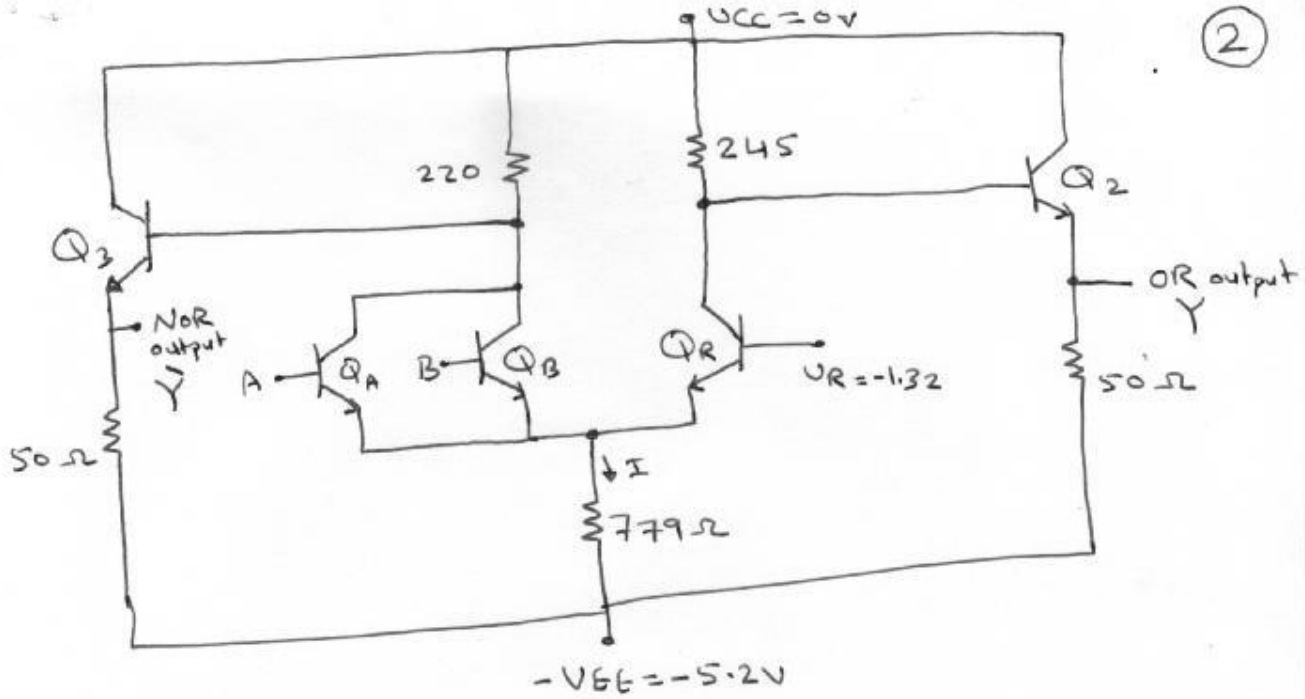
differential amplifier (Basic element of the ECL family).

$V_{OH} = V_{CC}$

$V_{OL} = V_{CC} - I R_C$



ECL basic gate (OR and NOR



Simplified ECL in order to calculate the output voltage levels

At output Y (OR output) :-

(a) If all inputs (A and B in this case) are low then assume Q_A and Q_B are off and Q_R is conducting.

$$V_E = -1.32 - 0.7$$
$$= -2.02\ V$$

$$I = \frac{-2.02 + 5.2}{779} = 4.08\ mA.$$

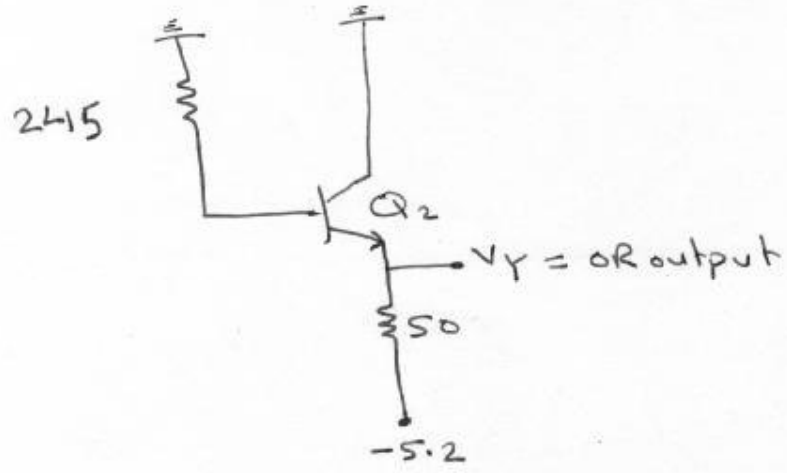
$$V_Y = -0.245 * I - V_{BE_2}$$
$$= -0.245 * 4.08 - 0.7$$
$$= -1.7\ V = V(0)$$

If A and B are at $V(0) = -1.7\,V$ and $V_E = -2.02\,V$

then V_{BE_A} and $V_{BE_B} = -1.7 + 2.02 = 0.32$

then Q_A and Q_B are not conducting

*If at least one of the inputs is high then its corresponding transistor (Q_A or Q_B) is conducting and Q_R is off.



assume $\beta_2 = 100$

$$I_B * 245 + 0.7 + 50 * I_E = 5.2$$

$$I_B * 245 + 0.7 + 50 * I_B(1+100) = 5.2$$

$$I_B = 0.85\ mA.$$

$$V_Y = -0.908 = V(1) = V_H$$

when all inputs (inputs A and B in this case) are high at $V(1) = -0.908$

then $V_E = -0.908 - 0.7 = -1.608\ V$

$$I = \frac{-1.608 + 5.2}{0.779K} = 4.6mA .$$

The emitter followers shift the level of the output signals by one V_{BE} drop. These shifted levels are needed in order that one gate can drive another. This compatibility of logic levels at input and output is an essential requirement in the design of gate circuits.

ECL advantages

1- High speed, the highest of all logic families since transistors do not saturate.

2- Complementary outputs are available which simplifies the logic design.

3- The differential nature of the circuit makes it less effected by noise.

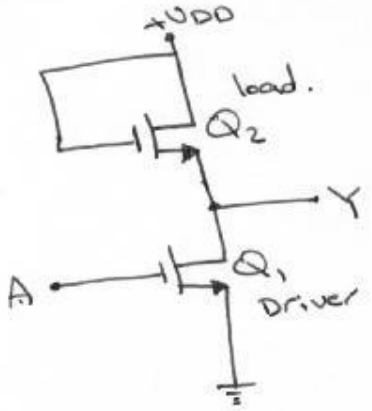
ECL disadvantages:-

① The power dissipation is high as compared to other logic families.

MOSFET

* MOSFET circuits are slower than corresponding BJT circuits because of the parasitic capacitance.
* The lower power dissipation and higher packing density of MOS devices make them more attractive and economical.

MOSFET Inverter:-

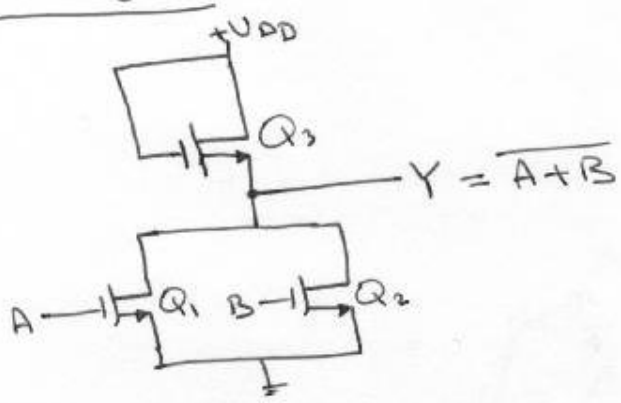


A	Y
VDD	0
0	VDD

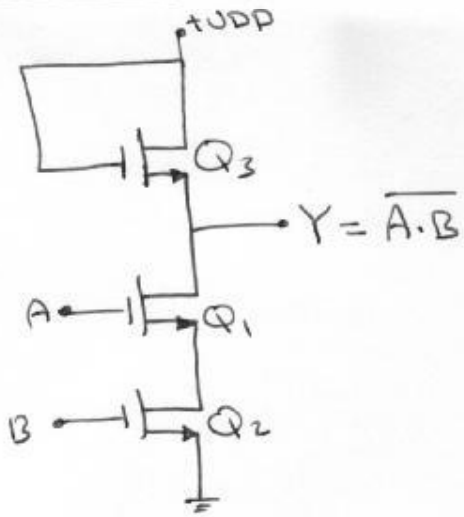
$Y = \bar{A}$

MOSFET Logic gates:-

NOR gate:-



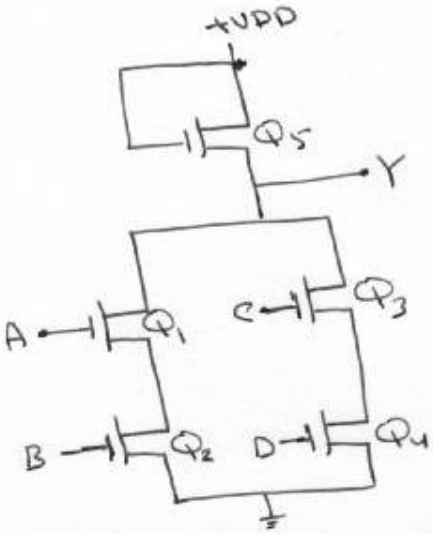
NAND gate:-



Example:-

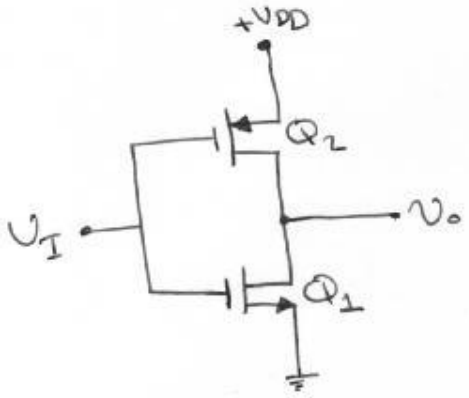
Implement the following function using NMOS logic.

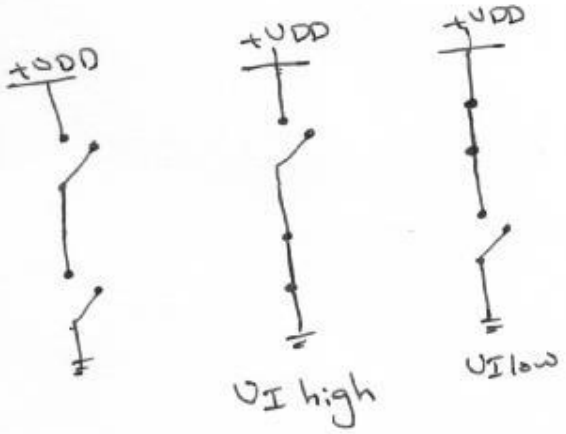
$Y = \overline{AB + CD}$



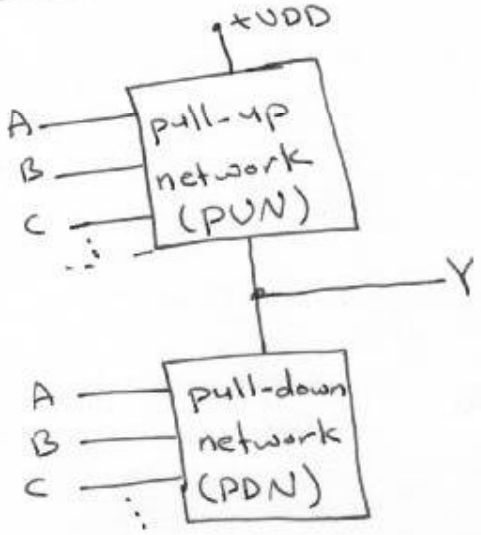
CMOS technology (complementary metal oxide semiconductor)

CMOS Inverter:-



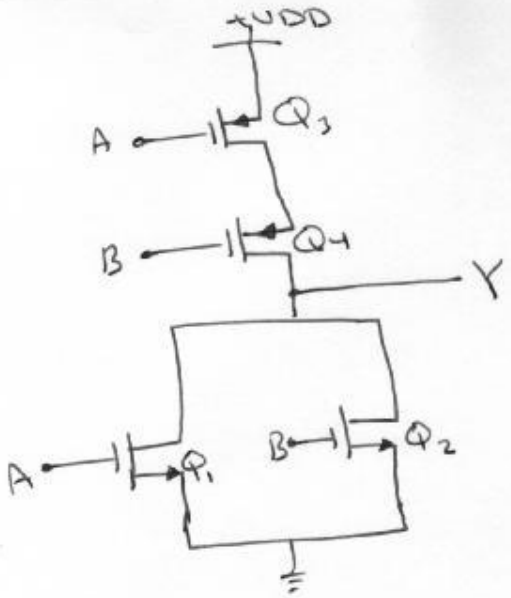


Basic structure of CMOS Logic Circuits:-



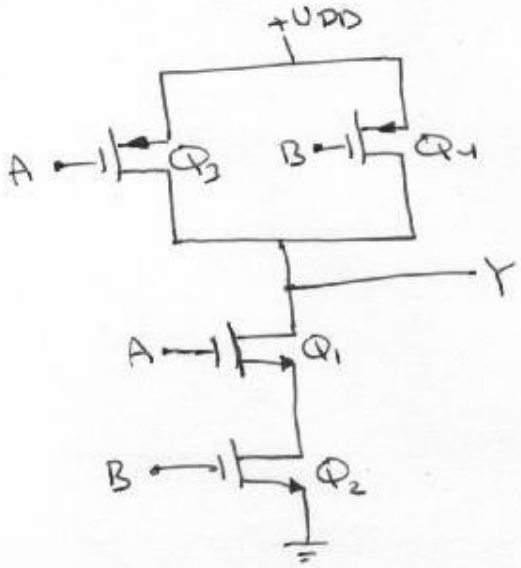
* PDN is constructed from only NMOS transistors, thus PDN is activated when the inputs are high.
* PUN is constructed from only PMOS transistors, thus PUN is activated when the inputs are low.

CMOS NOR gate:-



$$Y = \overline{A+B} = \bar{A}\,\bar{B}$$

CMOS NAND gate:-



$$Y = \overline{AB} = \bar{A}+\bar{B}$$

Example:-

Realize the following logic function using CMOS logic.

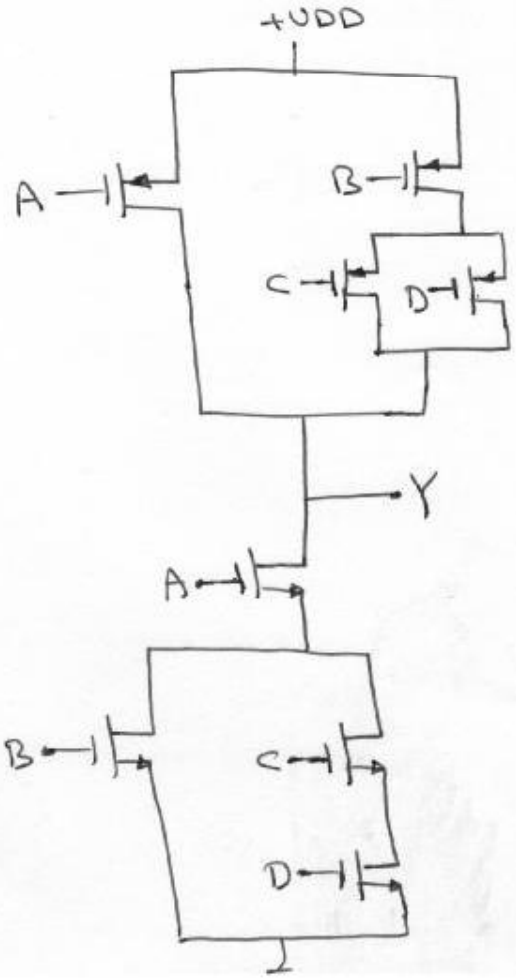
$$Y = \overline{A(B+CD)}$$

Sol.:-

$\bar{Y} = A(B+CD)$ from which PDN is obtained

To obtain the PUN

$$Y = \overline{A(B+CD)}$$
$$Y = \bar{A} + \overline{(B+CD)} = \bar{A} + \bar{B}.\overline{CD}$$
$$Y = \bar{A} + \bar{B}.(\bar{C}+\bar{D}).$$



Example:-

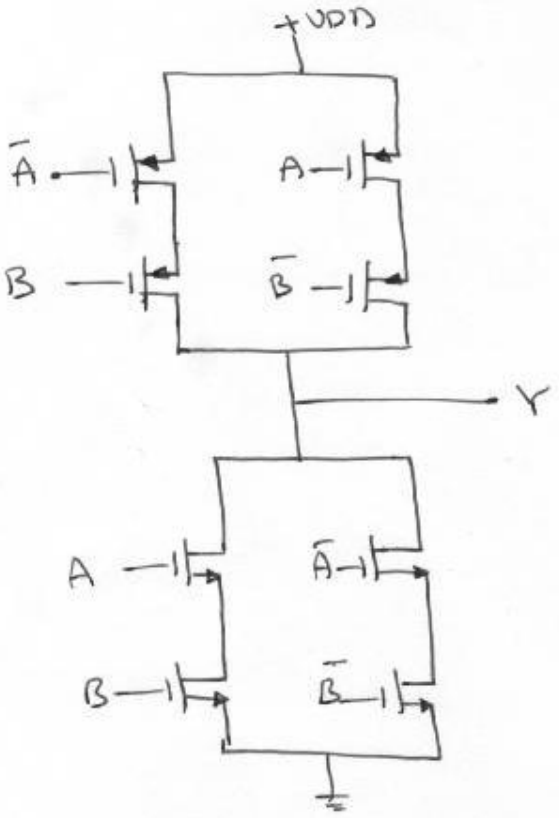
Realize the Exclusive-OR Function:-

$Y = A\bar{B} + \bar{A}B$ using CMOS logic.

Sol.:-

$Y = A\bar{B} + \bar{A}B$ from which PUN is obtained

$\bar{Y} = AB + \bar{A}\bar{B}$



Using direct method

H.w/ Solve the same example using the duality property.

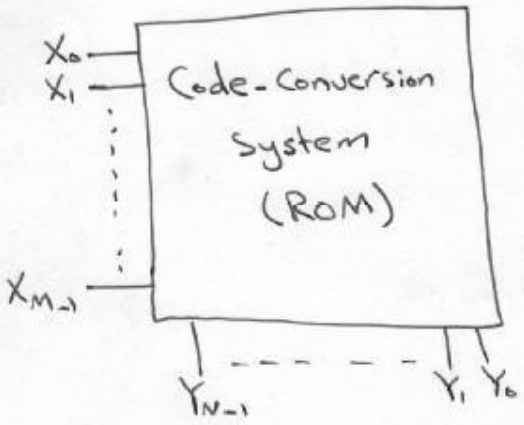
Semiconductor Memories:-

1- Read only Memory : (ROM)

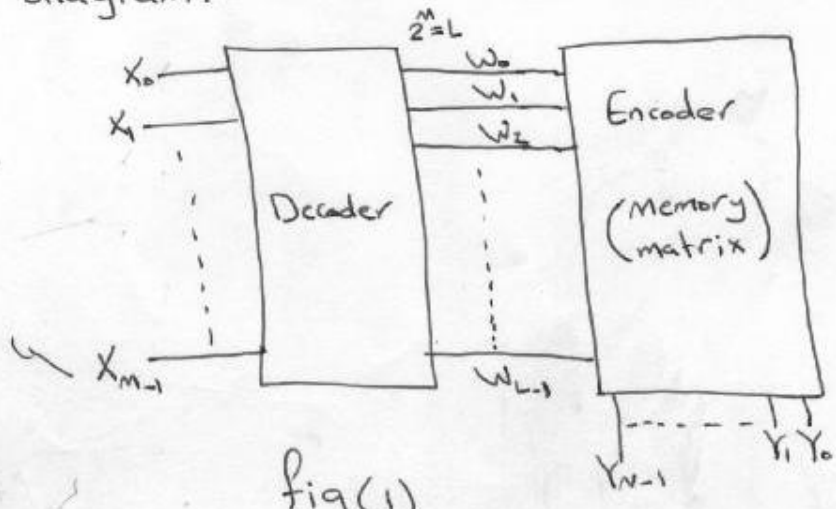
ROM is a memory that can be viewed as a combinational Logic circuit that contains fixed data patterns.

A ROM is a nonvolatile memory, meaning that the data is not lost with power supply switch off.

A ROM can be considered as a code-conversion system as in the following block diagram:-



which can be achieved as in the following block diagram:-



fig(1)

Consider a 64-bit ROM arranged in 16 words of 4-bit each.

X_3	X_2	X_1	X_0	word line	Y_3 Y_2 Y_1 Y_0 (o/p as required)
0	0	0	0	W_0	
0	0	0	1	W_1	
0	0	1	0	W_2	
0	0	1	1	W_3	
				⋮	as required
1	1	1	1	W_{15}	

Two-Dimensional addressing of a ROM

For a ROM with a large size, the previous decoding arrangment in fig(1) is impractical. The number of gates in the decoder becomes very large. Therefore 2-D addressing (X,Y) addressing is used.

Example:-

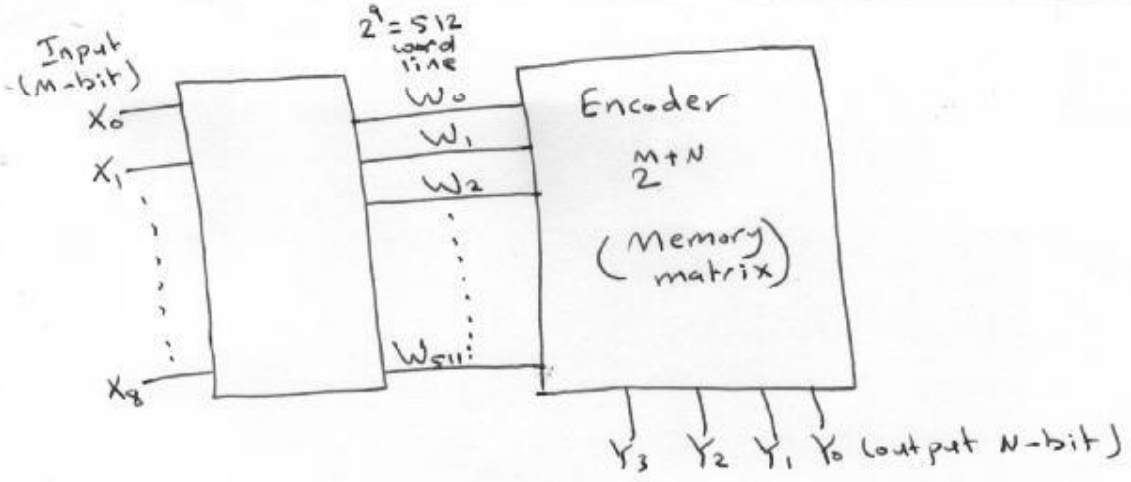
2048-bit (2Kb) with 4-output lines ROM

Sol:-

if the block arrangement of fig(1) is used then

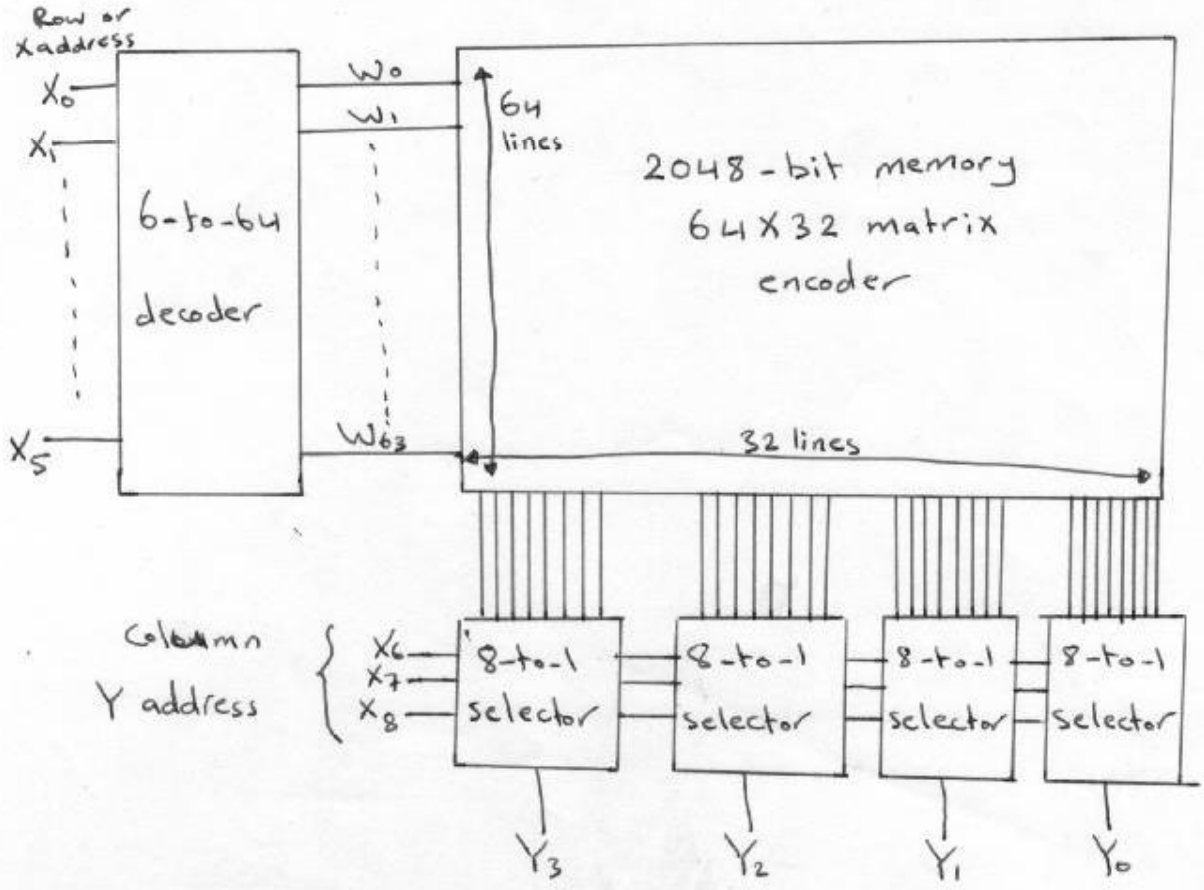
$2048 = 2^{11} = 2^9 * 2^2$

$M = 9,\ N = 4$



The decoder circuit will require 512 gates (1 for one each word line) which is impractical.

Therefore this 2-Dimensional addressing arrangment is used:-



A 6-bit row address or X address is used which results in 64 word lines (horizontal lines). (4)

If 32 vertical lines are used in the memory matrix which results in $64 \times 32 = 2048$ bits.

However, only four output lines are specified then four 8-to-1 line selectors are used. A 3-bit column address feeds each multiplexer.

Row address Decoder

As an example let us take $M = 3$ with the three address bits denoted X_0, X_1, and X_2 and the 8-word lines denoted $W_0, W_1, \ldots W_7$.

From the truth table we can construct the Row address decoder in an array form using NMOS gates as in the following:-

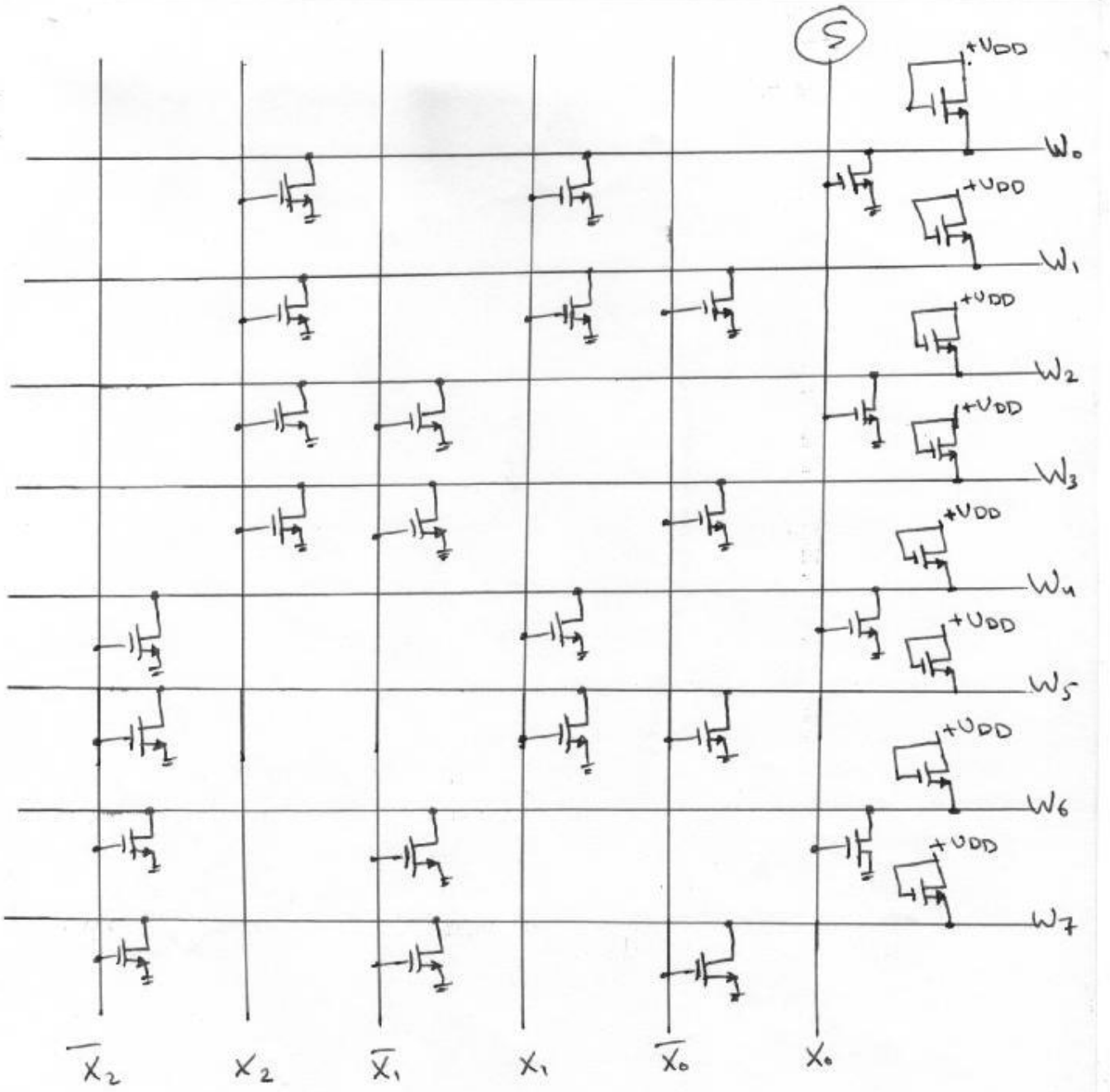
X_2	X_1	X_0	word line
0	0	0	W_0
0	0	1	W_1
0	1	0	W_2
0	1	1	W_3
1	0	0	W_4
1	0	1	W_5
1	1	0	W_6
1	1	1	W_7

$$W_0 = \overline{\overline{X_0}\,\overline{X_1}\,\overline{X_2}}$$

$$W_0 = \overline{X_0 + X_1 + X_2}$$

$$W_5 = \overline{\overline{X_0}\,\overline{X_1}\,X_2}$$

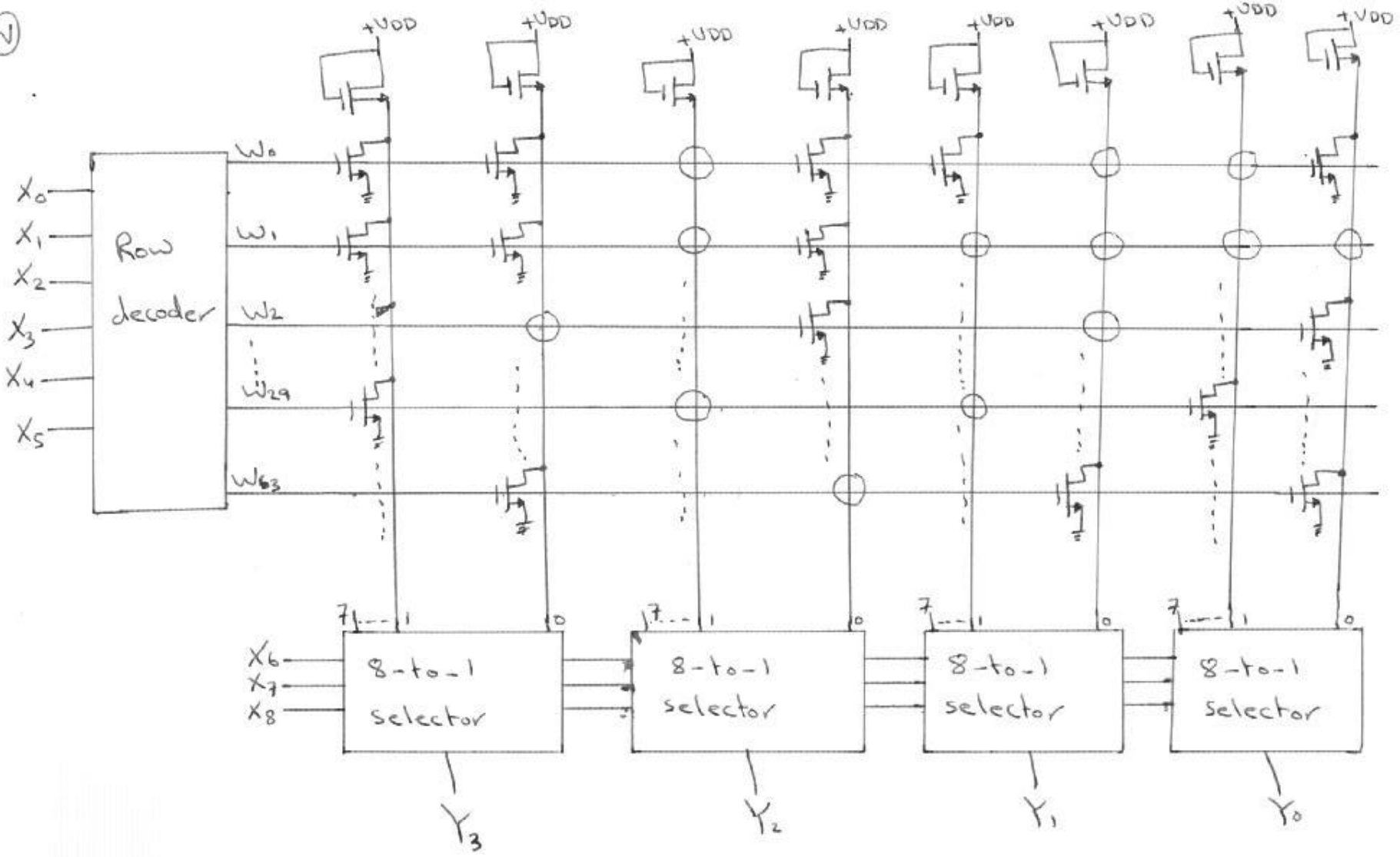
$$W_5 = \overline{\overline{X_0} + X_1 + \overline{X_2}}$$


S
+VDD
W0
W1
W2
W3
W4
W5
W6
W7
X̄2
X2
X̄1
X1
X̄0
X0

Memory matrix (encoder)

X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	word line	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0	0	W_0	0	0	1	0
0	0	0	0	0	0	0	0	1	W_1	0	0	1	1
0	0	0	0	0	0	0	1	0	W_2	1	0	1	0
0	0	0	1	1	1	1	1	1	W_{63}	0	1	0	0
0	0	1	0	0	0	0	0	0	W_0	0	1	0	1
0	0	1	0	0	0	0	0	1	W_1	0	1	1	1
0	0	1	0	1	1	1	0	1	W_{29}	0	1	1	0

(2)


+VDD
X0
X1
X2
X3
X4
X5
Row decoder
W0
W1
W2
W29
W63
7
1
0
X6
X7
X8
8-to-1 selector
Y3
Y2
Y1
Y0

Random Access Memory :- (RAM)

In a semiconductor memory an array of storage cells is used in constructing a RAM.

Eeach cell is holding 1 bit of data.
A RAM is a voltatile memory, which means that all stored information is lost when power supply is turned off.

Two- Dimensional addressing of a RAM :-

A great economy of the number of gates in the decoder circuit is obtained by arranging the memory cells in a two-dimensional array.

For example:- A 4k bit RAM is organized in a 64X64 array as in the following:-

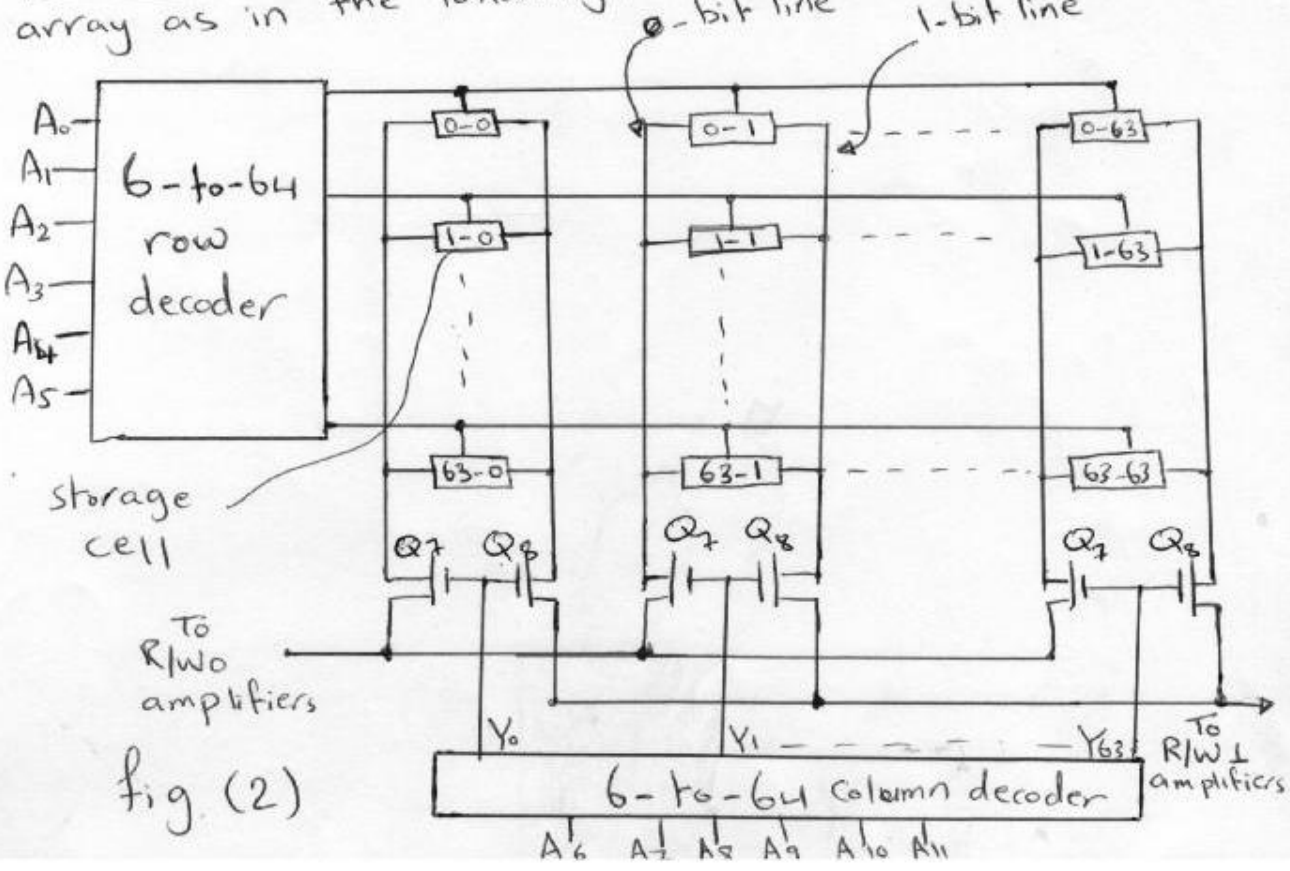
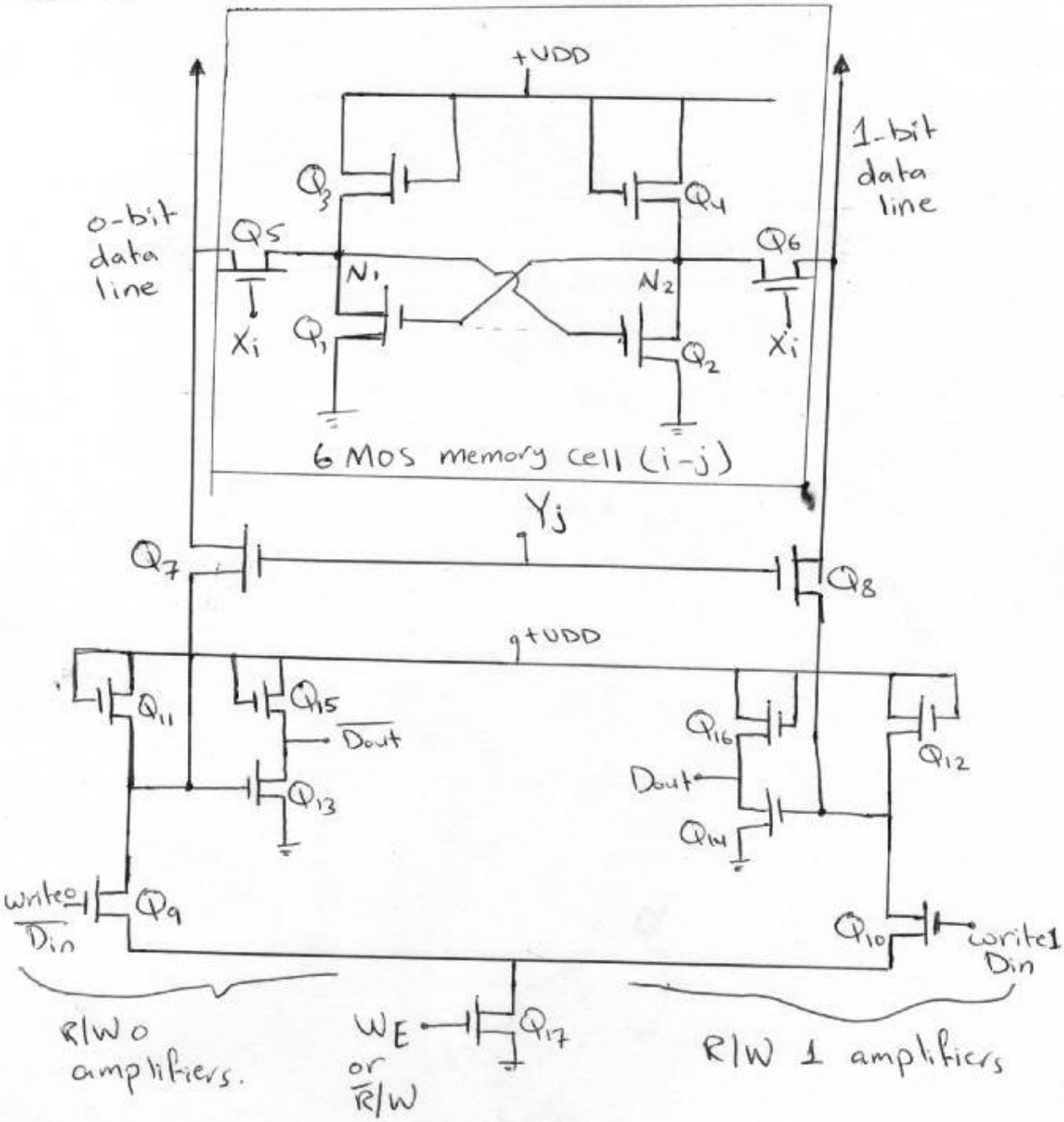


fig (2)

Figure (2) shows the organization of a 4096-word-by-1 bit RAM.

RAM cells :-

(a) Static MOS RAM



* To select a cell its x and y address should be excited (2-Dimensional) addressing.

* Q_{17} and Q_{10} form an AND gate with inputs W_E and D_{in}. also Q_{17} and Q_9 form an AND gate with inputs W_E and $\overline{D_{in}}$.

where W_E or $\overline{R/W}$ = write enable

D_{in} = Data input

D_{out} = Data output.

Case I

(write a 1 in the cell)

① address the cell ($X_i = 1$ and $y_j = 1$) so that Q_7, Q_8, Q_5 and Q_6 are conducting.

② set $W_E = 1$, $D_{in} = 1$ and $\overline{D_{in}} = 0$

* then Q_{17} and Q_{10} are ON and Q_9 is off. Hence the 1-bit data line is grounded and 0-bit data line goes to V_{DD} through load Q_{11}.

* Thus node N_2 is effectively grounded.

* So Q_1 is cutoff and N_1 rises to V_{DD}.

* N_1 is tied to the gate of Q_2 therefore Q_2 is held ON and N_2 is maintained at 0V.

* when the address is removed (Q_5, Q_6, Q_7 and Q_8 are off), Q_2 is ON, Q_1 is off, and a 1 has been written into the selected memory cell.

Case II (read a 1 stored in a memory cell)

① Set $X_i = 1$ and $Y_j = 1$

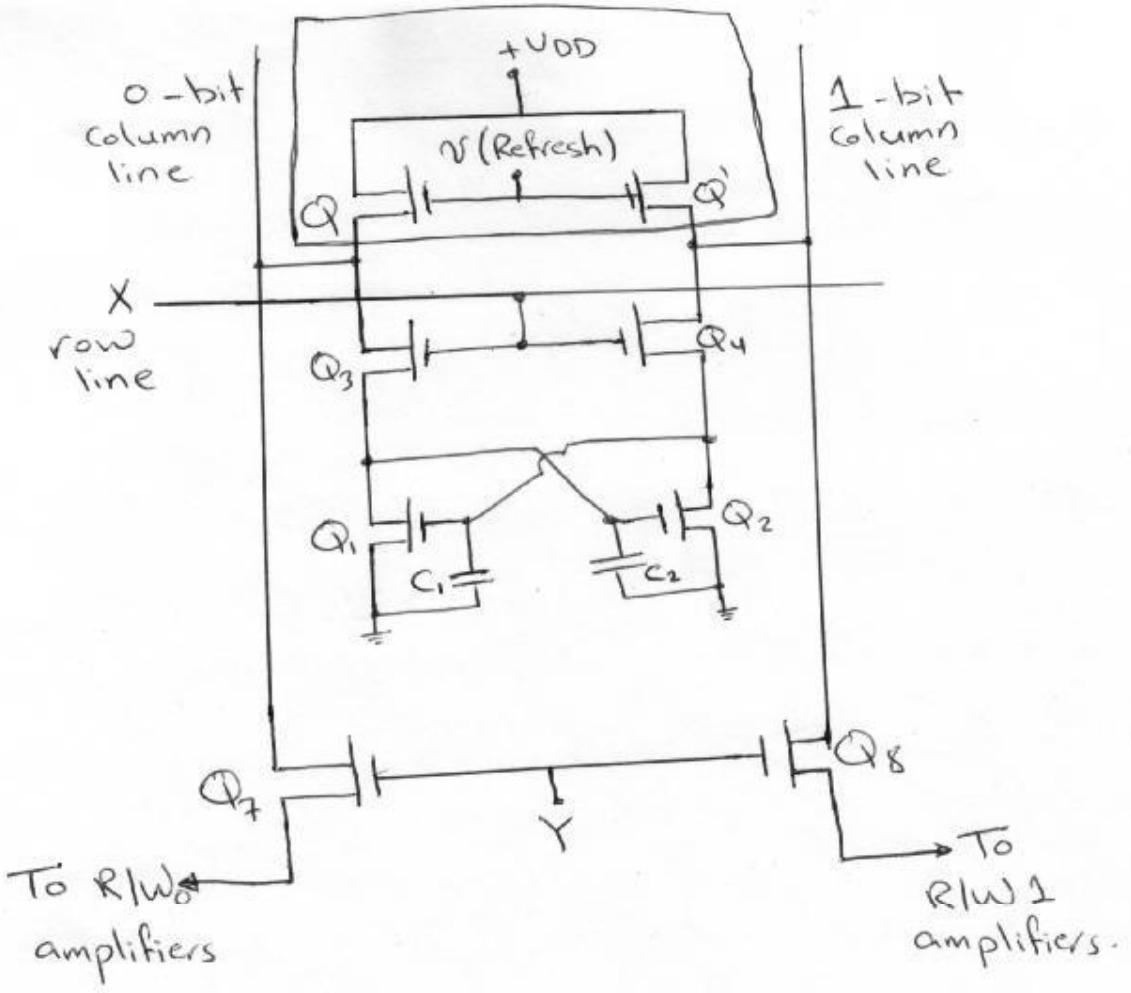
② assume that a 1 is stored in this cell so Q_2 is ON and Q_1 is OFF (N_2 is at 0V and N_1 is at V_{DD}).

③ Set $W_E = 0$.

* Then Q_{17} is off and hence Q_{10} and Q_9 are non conducting.
* So the 1-bit data line and the 0-bit data line are connected to V_{DD} through load Q_{12} and Q_{11} respectively.
* since Q_2 is ON (N_2 at 0V) then the 1-bit line is effectively grounded.
* therefore Q_{14} is off and Dout $= V_{DD}$ (logic 1).
* Since Q_1 is off then 0-bit data line is at V_{DD}.
* therefore Q_{13} is ON and $\overline{\text{Dout}} = 0$

So we have read 1 stored in cell (i, j).

Dynamic RAM cell:-



In the Dynamic RAM cell, information is stored as charge on the two capacitors C_1 and C_2.

If a 1 is written in the cell then C_2 is charged to V_{DD} and C_1 is charged to 0 volt, so that Q_2 is ON and Q_1 is off.

In DRAM the capacitors which store the information will discharge slowly because of the leakage currents and information may be lost.

Therefore DRAM require periodic refreshing to regenerate the data stored on capacitors.

The two transistors (Q and Q') are added to refresh each cell in a given column.

If we have a RAM with 64 columns then 64 of such circuitry (Q and Q') is needed to refresh a cell in that column.

v is a pulse of less than 1 Msec occurring about every 2 msec.

If X_1 is high and v is also high then row(1) will be refreshed simultaneously.

Because X_1 is high then Q_3 and Q_4 are ON, and because v (Refresh) is high then Q and Q' are ON.

Assume that Q_1 is off and Q_2 is ON (storing a 1). Then during the refresh interval a current will flow in Q and Q_3 charging C_2 toward V_{DD} and since Q_1 is off all the current from V_{DD} is directed toward C_2.

As for the current in Q' and Q_4 then C_1 will not be charged because Q_2 is conducting. So the cell is restored to its original state.